JM70 -MV Block Diagram

Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246

CLK GEN.
ICS9LPRS365BKLFT 3

Mobile CPU
Penryn 4, 5

SMSC
EMC2102 38

HOST BUS 667/800/1066MHz@1.05V

DDR3 800/1066 MHz 16,17

DDR3 800/1066 MHz 16,17

Cantiga 6,7,8,9,10,11
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F

PCIex16

VGA Borad 18
(MXM 3.0 Connector)

Level shift
PS8101

HDMI 21

LCD 19

CRT 20

X4 DMI 400MHz

C-Link0

ICH9M 12,13,14,15
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)

USB

CardBus
AU6433 35

MS/MS Pro/xD
/MMC/SD 35

LAN
Giga LAN
BCM5764MKMLG 28

TXFM 29

RJ45 29

New Card 36

PWR SW
TPS2231 36

PCIe

Mini 1 Card
Wire LAN 37

Mini 2 Card
TV TUNER 37

LPC BUS

AZALIA

32 INT.SUBWOOFER

SUBWOOFER
AMP
G1442RD 32

LINE IN 32

Int MIC 32

Codec
ALC888 30

MIC In 32

32 INT.SPKR 1.5W

OP AMP
G1454R 31

32 Line Out (SPDIF)

RJ11

MODEM
MDC Card 34

SATA

HDD SATA 22

SATA

ODD SATA 24

SATA

ESATA 25

SATA

2nd HDD 23

USB

Mini USB
Blue Tooth 26

Finger
Printer 41

Camera 19

USB
4 Port 27

KBC
Winbond
WPCE773LA0DG 39

SPI

BIOS
(2MB) 40

MEDIA
KEY 42

Touch
Pad 41

INT.
KB 39

LPC
DEBUG
CONN. 40

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

SYSTEM DC/DC ISL62392 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 46	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)

RT9026 49	
1.5V_S3	DDR_VREF_S3 (1.2A)

G9198-15 14	
3D3V_S5	1D5V_S5 (300mA)

CHARGER ISL88731A 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3208C 51	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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Title: Reference
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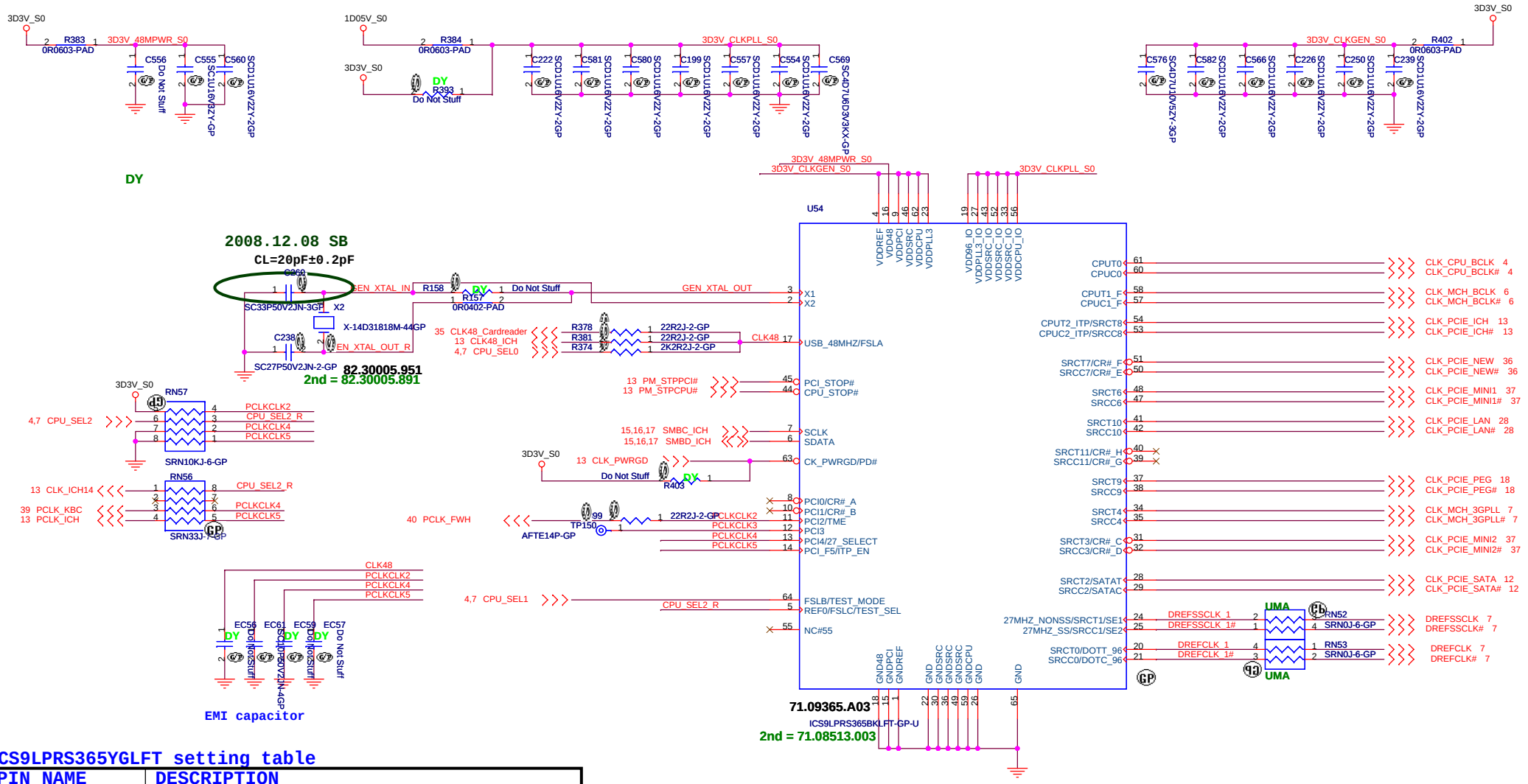

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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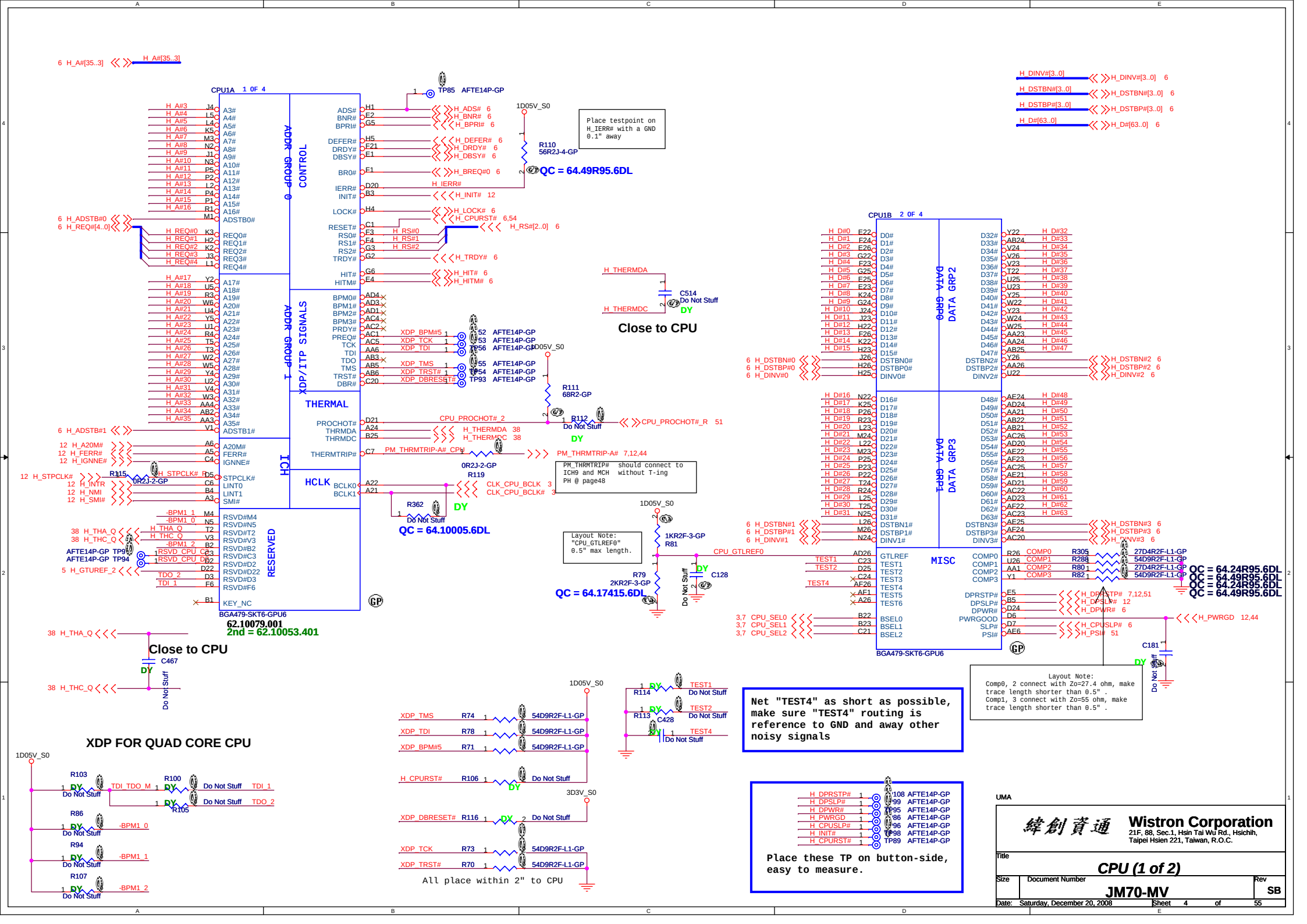
CPU1A 1 0F 4
BGA479-SKT6-GPU6
62.10079.001
2nd = 62.10053.401
CPU1B 2 0F 4
BGA479-SKT6-GPU6
Close to CPU
Close to CPU
QC = 64.49R95.6DL
QC = 64.10005.6DL
QC = 64.17415.6DL
QC = 64.24R95.6DL
QC = 64.49R95.6DL
QC = 64.24R95.6DL
QC = 64.49R95.6DL
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
XDP FOR QUAD CORE CPU
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UMA
CPU (1 of 2)
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Rev SB
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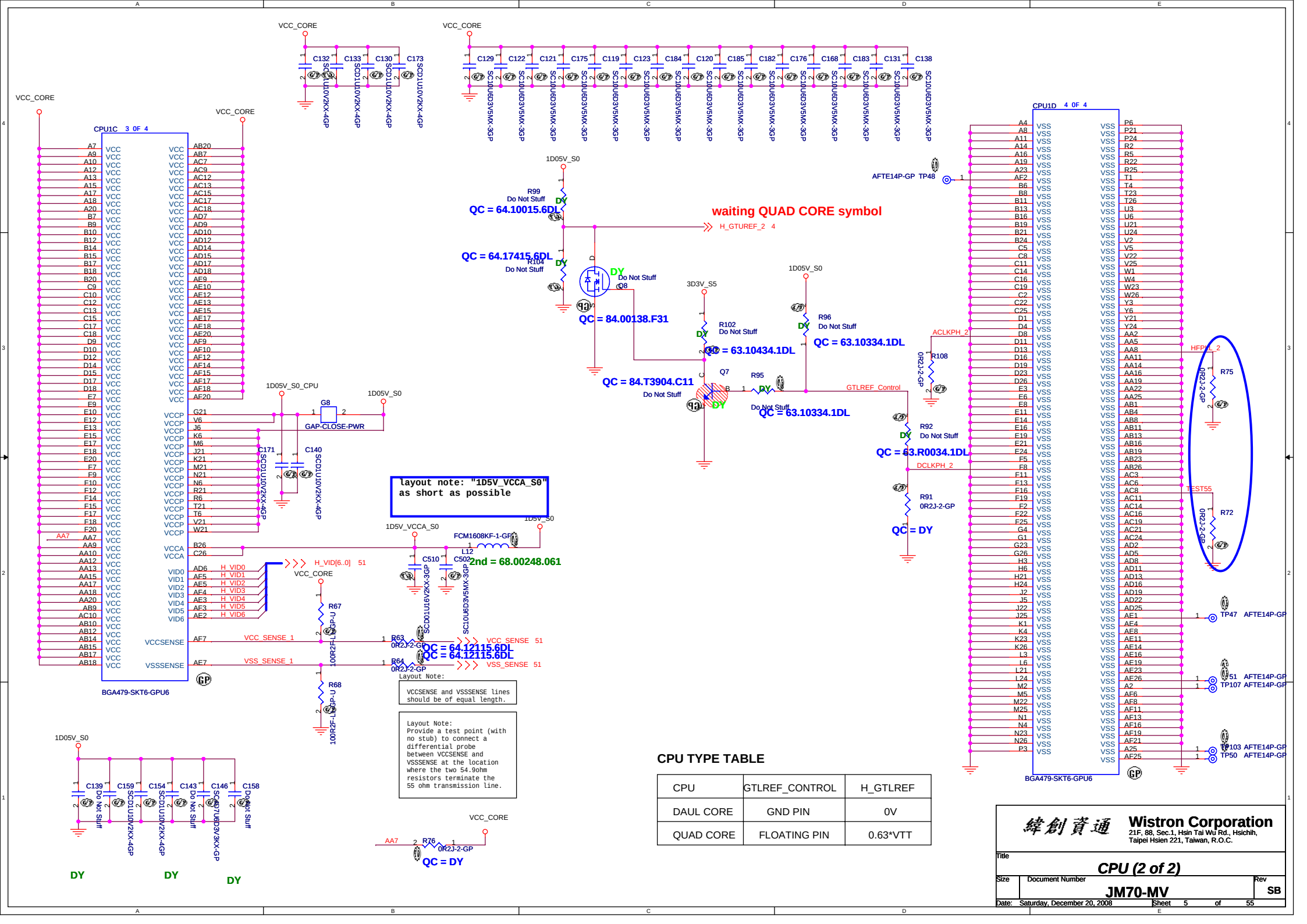

CPU TYPE TABLE

CPU	GTLREF_CONTROL	H_GTLREF
DAUL CORE	GND PIN	0V
QUAD CORE	FLOATING PIN	0.63*VTT

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Title	CPU (2 of 2)
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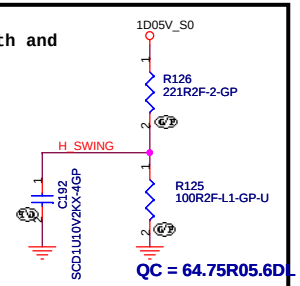
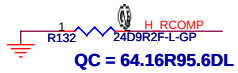
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



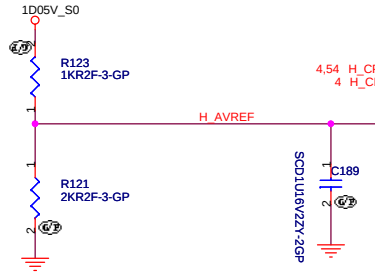
QC = 64.75R05.6DL

H_RCOMP routing Trace width and Spacing use 10 / 20 mil



QC = 64.16R95.6DL

Place them near to the chip (< 0.5")



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Title	Cantiga (1 of 6)	
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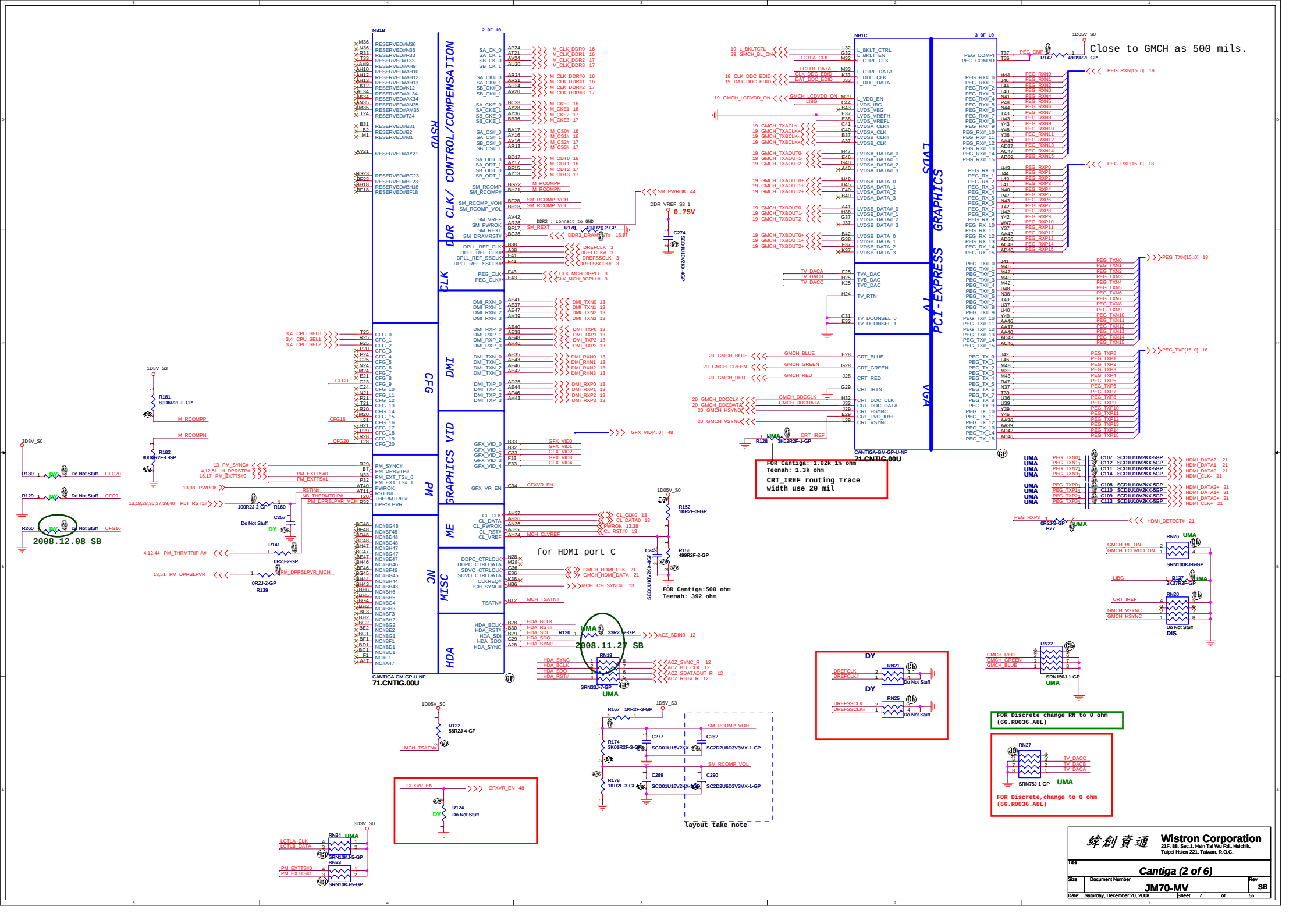
Close to GMCH as 500 mils.
2008.12.08 SB
2008.11.27 SB
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change RN to 0 ohm
(66.R0036.A8L)
FOR Discrete,change to 0 ohm
(66.R0036.A8L)
layout take note
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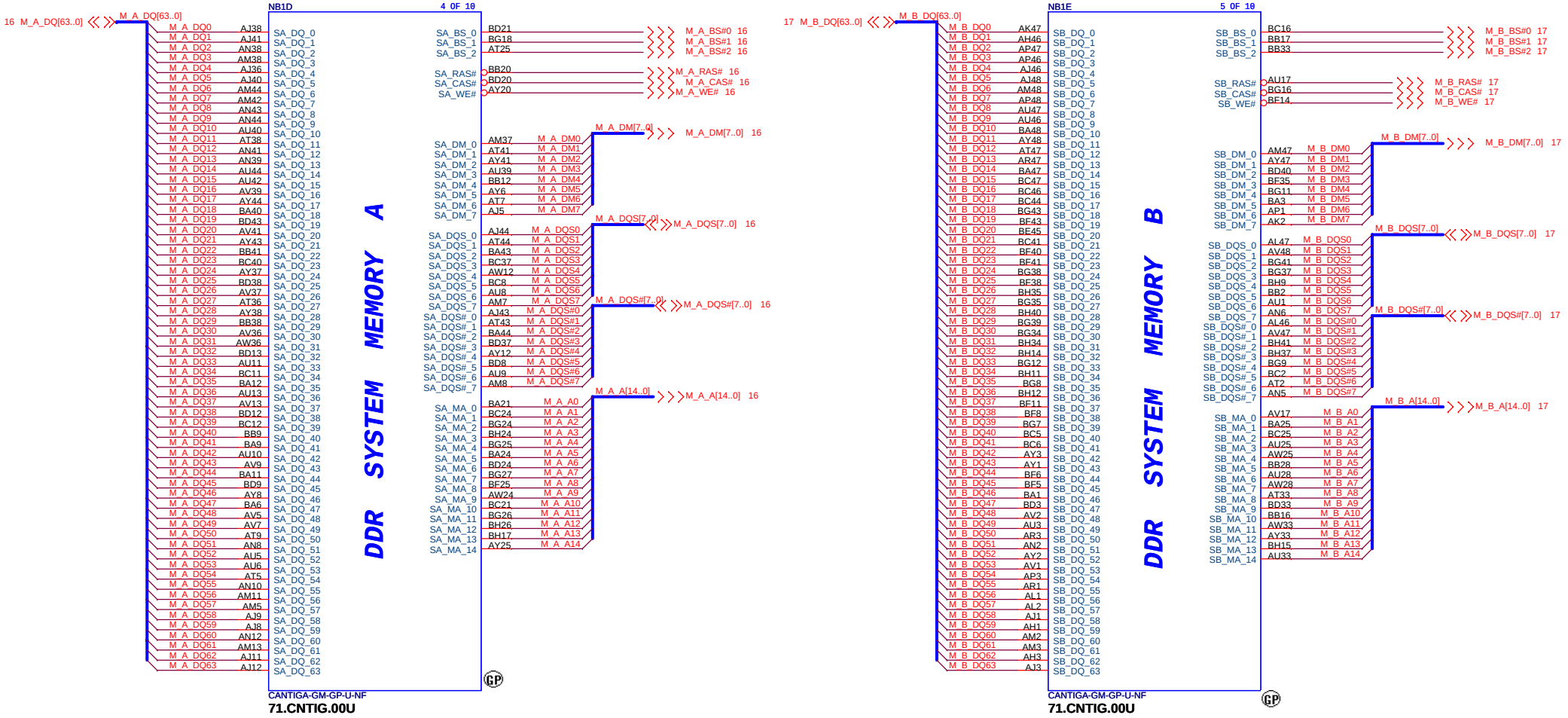
Cantiga (2 of 6)
JM70-MV
SB
Saturday, December 20, 2008



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Title: ***Cantiga (3 of 6)***

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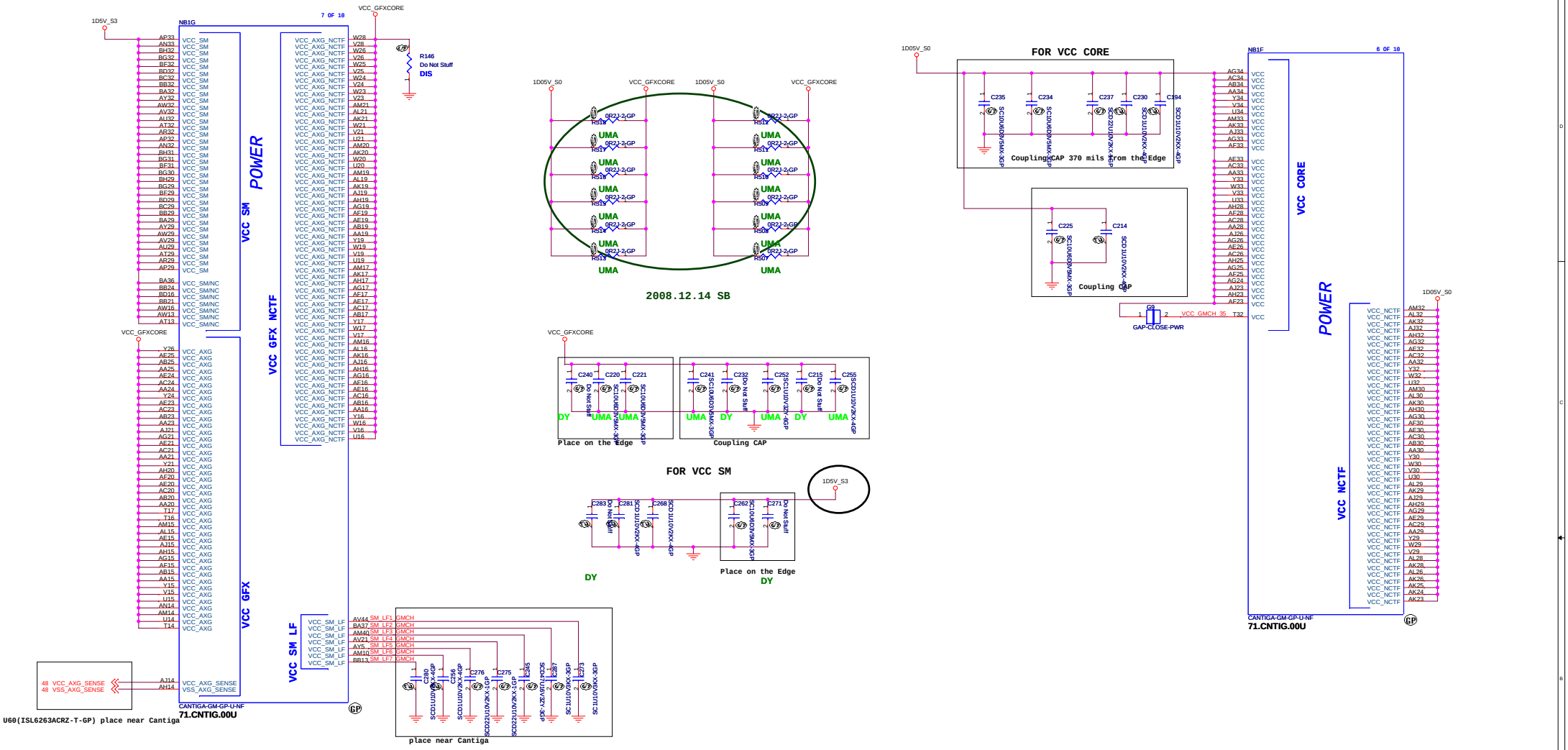

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Title	***Cantiga (4 of 6)***	
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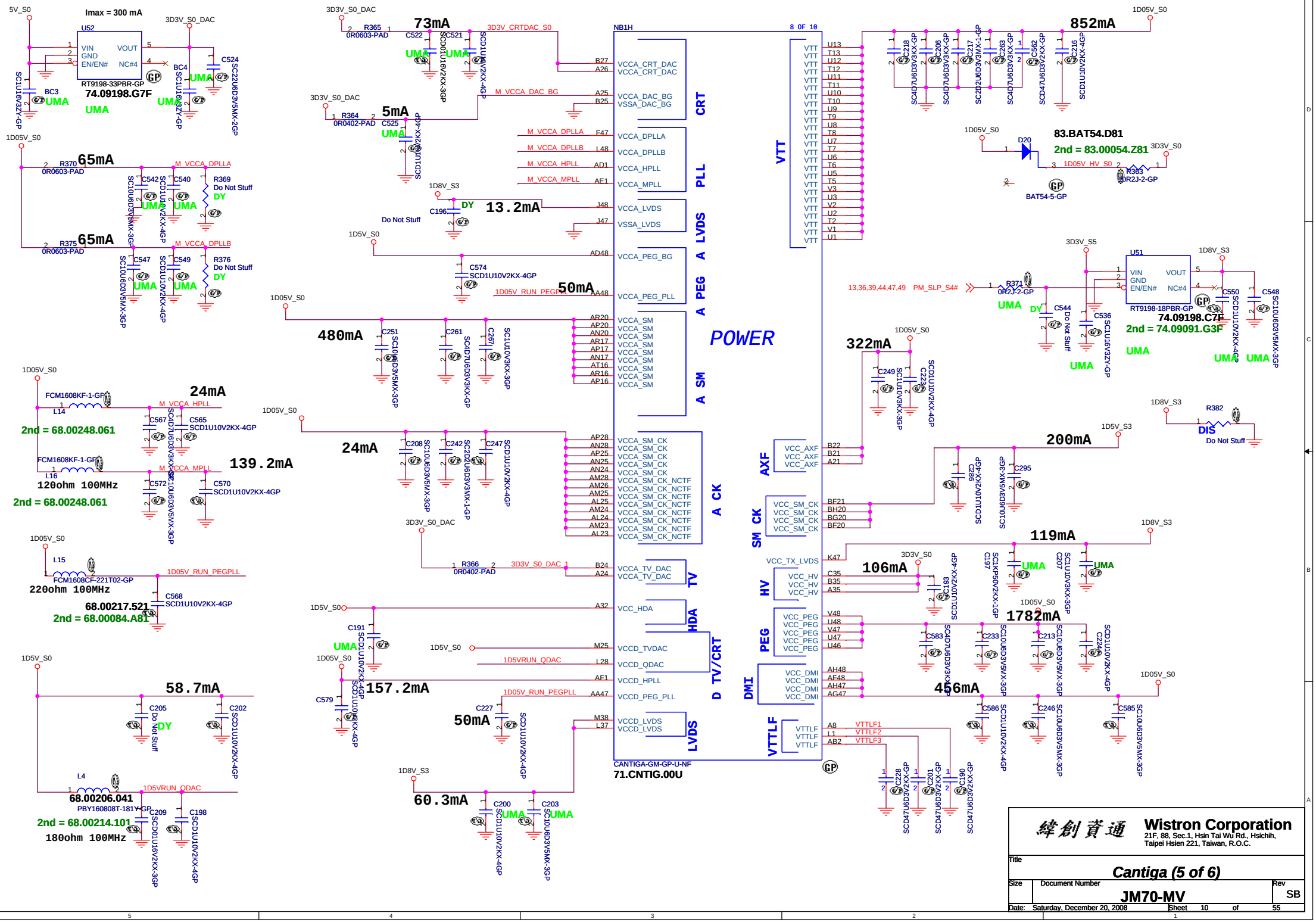
POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
74.09198.G7F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
58.7mA
157.2mA
50mA
60.3mA
852mA
83.BAT54.D81
2nd = 83.00054.Z81
322mA
74.09198.C7F
2nd = 74.09091.G3F
200mA
119mA
106mA
1782mA
456mA
24mA
2nd = 68.00248.061
68.00217.521
2nd = 68.00084.A81
68.00206.041
2nd = 68.00214.101
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Cantiga (5 of 6)
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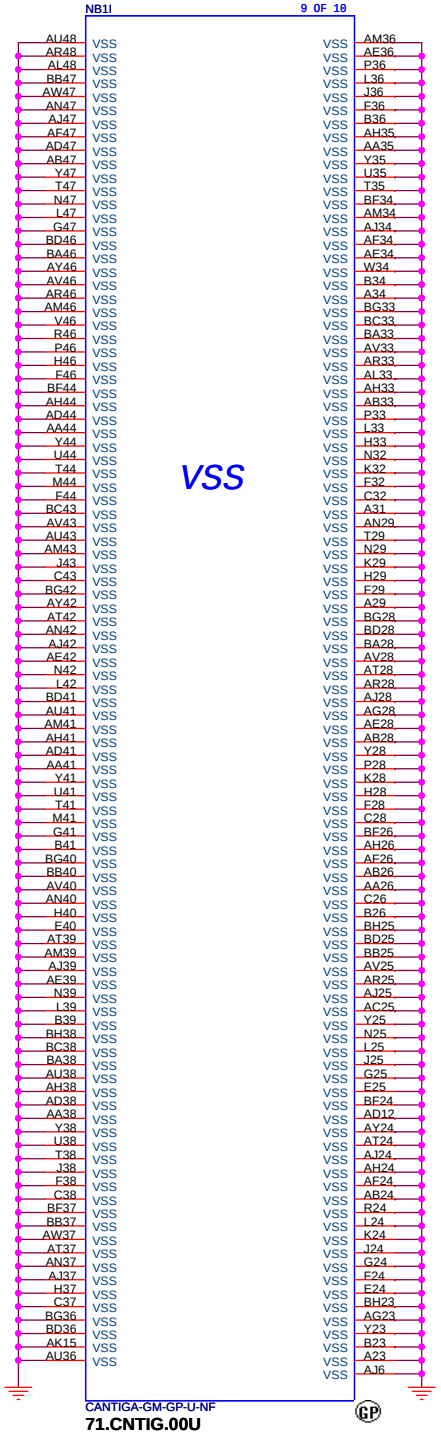

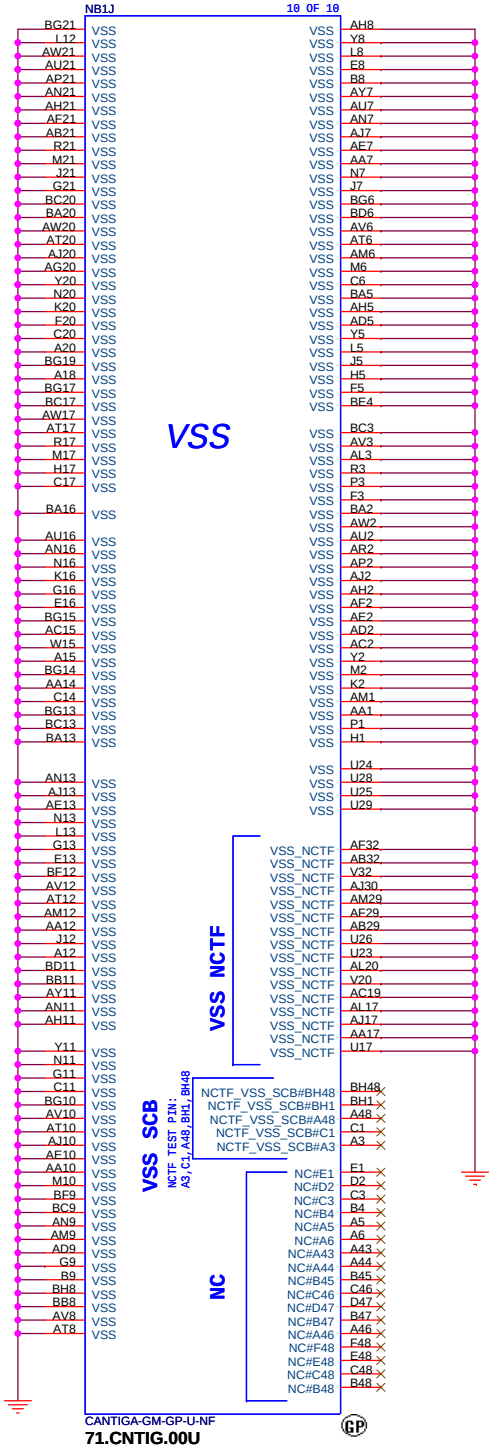

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Title	***Cantiga (6 of 6)***	
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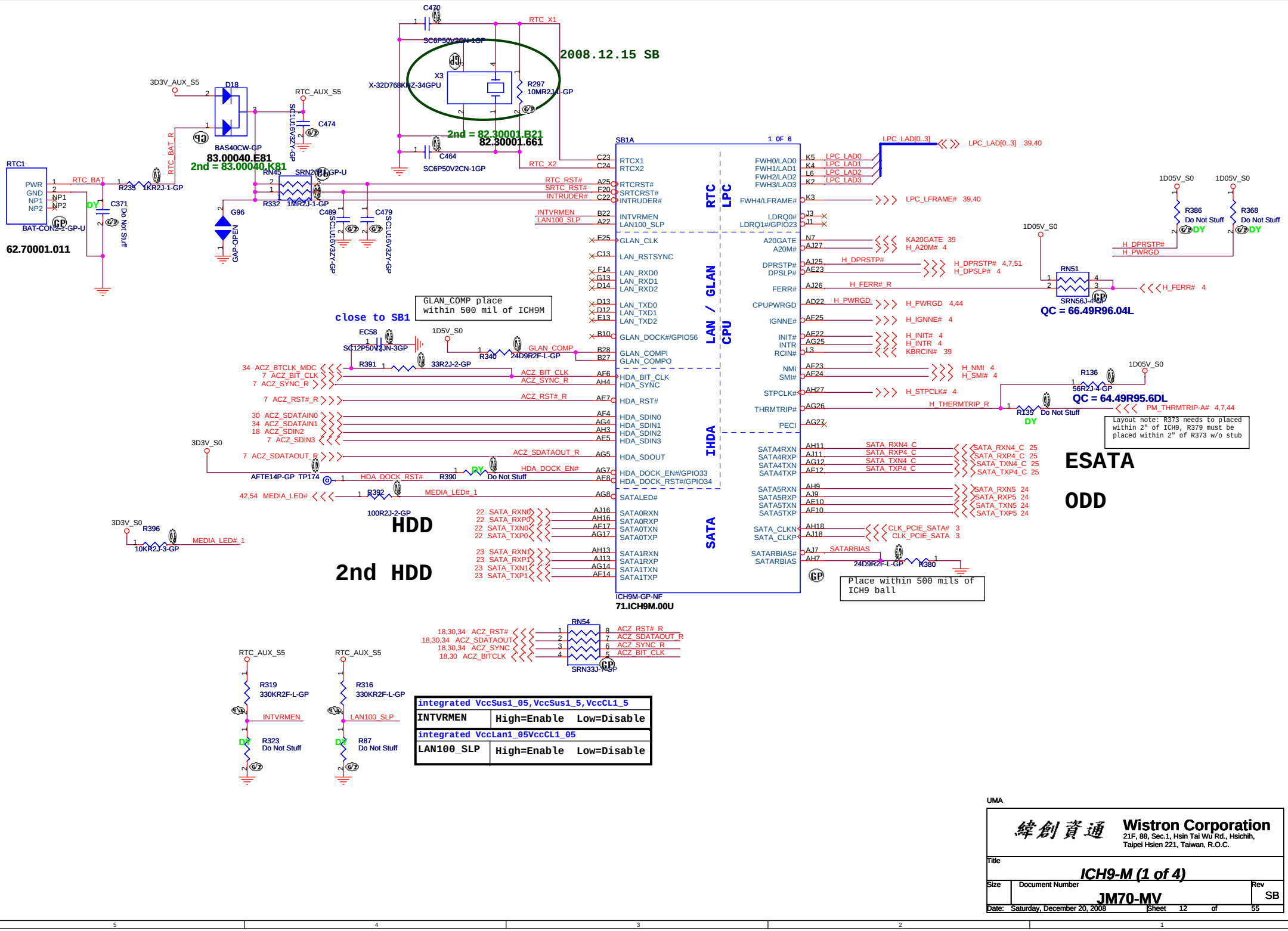
2008.12.15 SB
SB1A
1 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
HDD
2nd HDD
ESATA
ODD
close to SB1
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
QC = 66.49R96.04L
QC = 64.49R95.6DL
62.70001.011
83.00040.E81
2nd = 83.00040.K81
82.30001.661
2nd = 82.30001.B21
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
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Title
ICH9-M (1 of 4)
Size
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PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

These R need close SB
within 600 mils

SB1B 2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U

SB1C 3 OF 6
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U

SB1D 4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U

LAN
MINICARD1
MINICARD2
TV_tuner
TV_tuner
2008.12.14 SB
NEW
NEW
NEW CARD
2008.12.14 SB

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

2nd = 83.00016.F11 / 83.00016.G11
2nd = 83.00054.Z81
83.BAT54.D81
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Title: ICH9-M (2 of 4)
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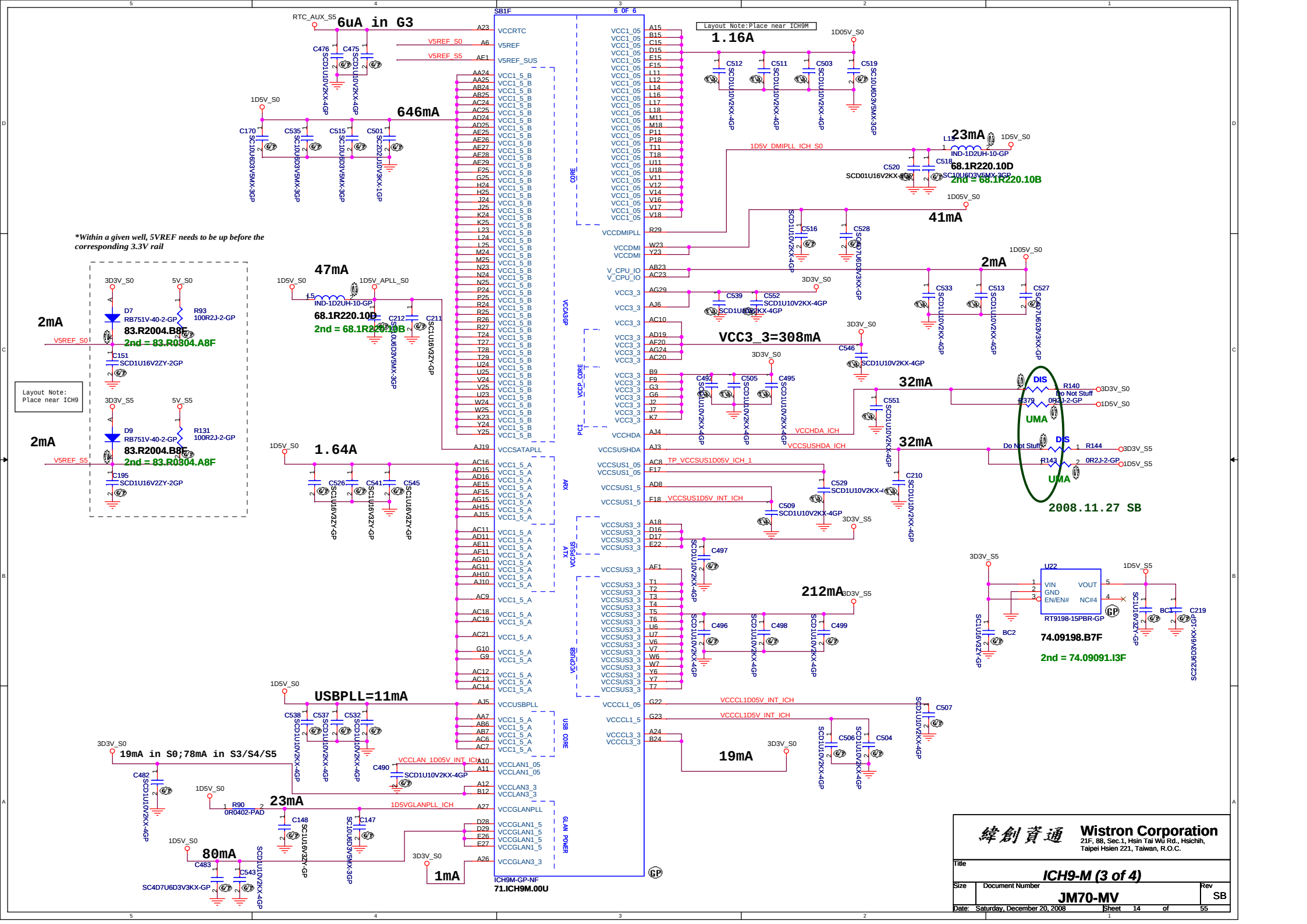
6uA in G3
1.16A
23mA
41mA
2mA
VCC3_3=308mA
32mA
32mA
646mA
47mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
212mA
19mA
2mA
2mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
DIS
UMA
DIS
UMA
Do Not Stuff
Do Not Stuff
2008.11.27 SB
68.1R220.10D
2nd = 68.1R220.10B
83.R2004.B8F
2nd = 83.R0304.A8F
83.R2004.B8F
2nd = 83.R0304.A8F
74.09198.B7F
2nd = 74.09091.I3F
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RT9198-15PBR-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
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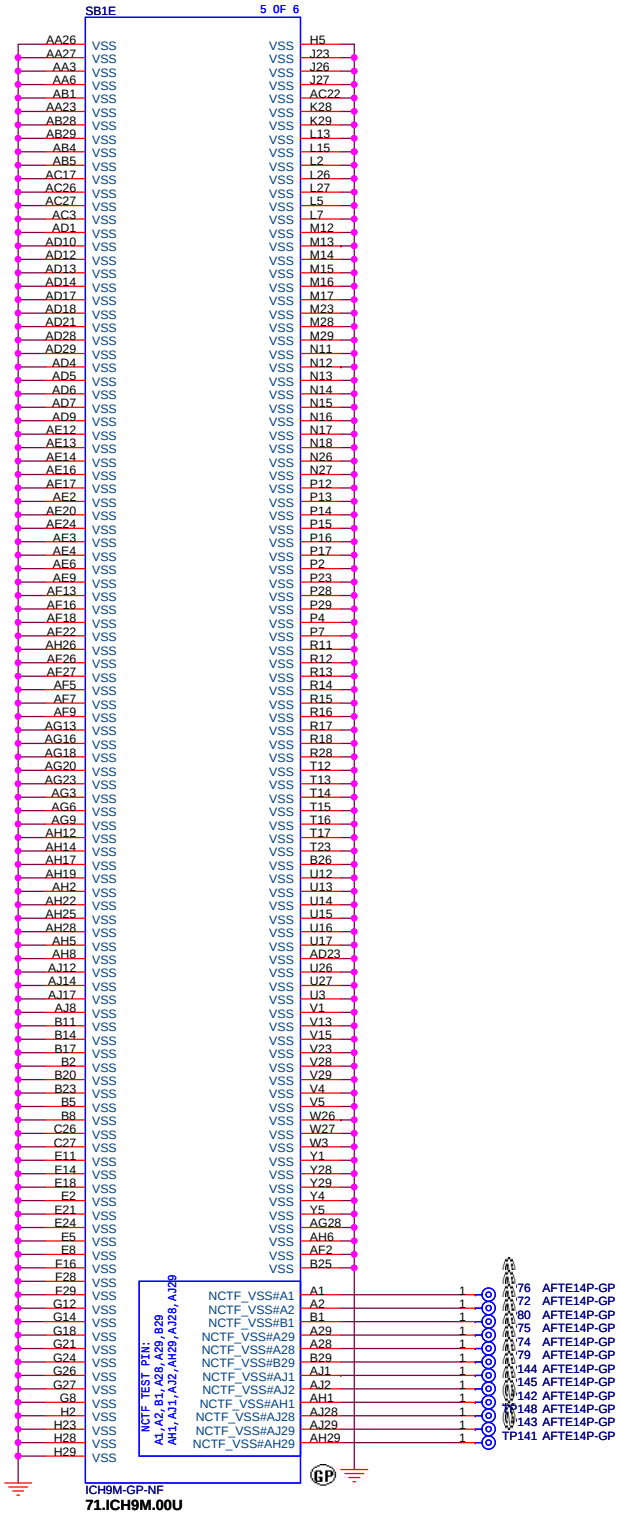
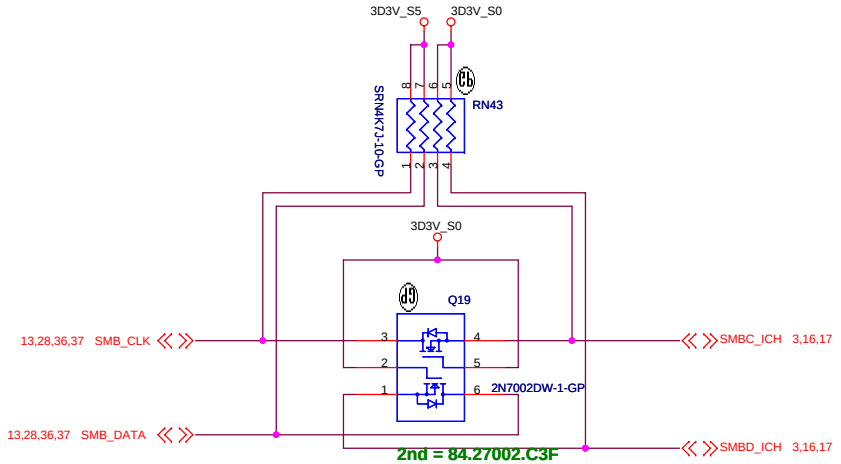
55





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*ICH9-M (4 of 4)*	
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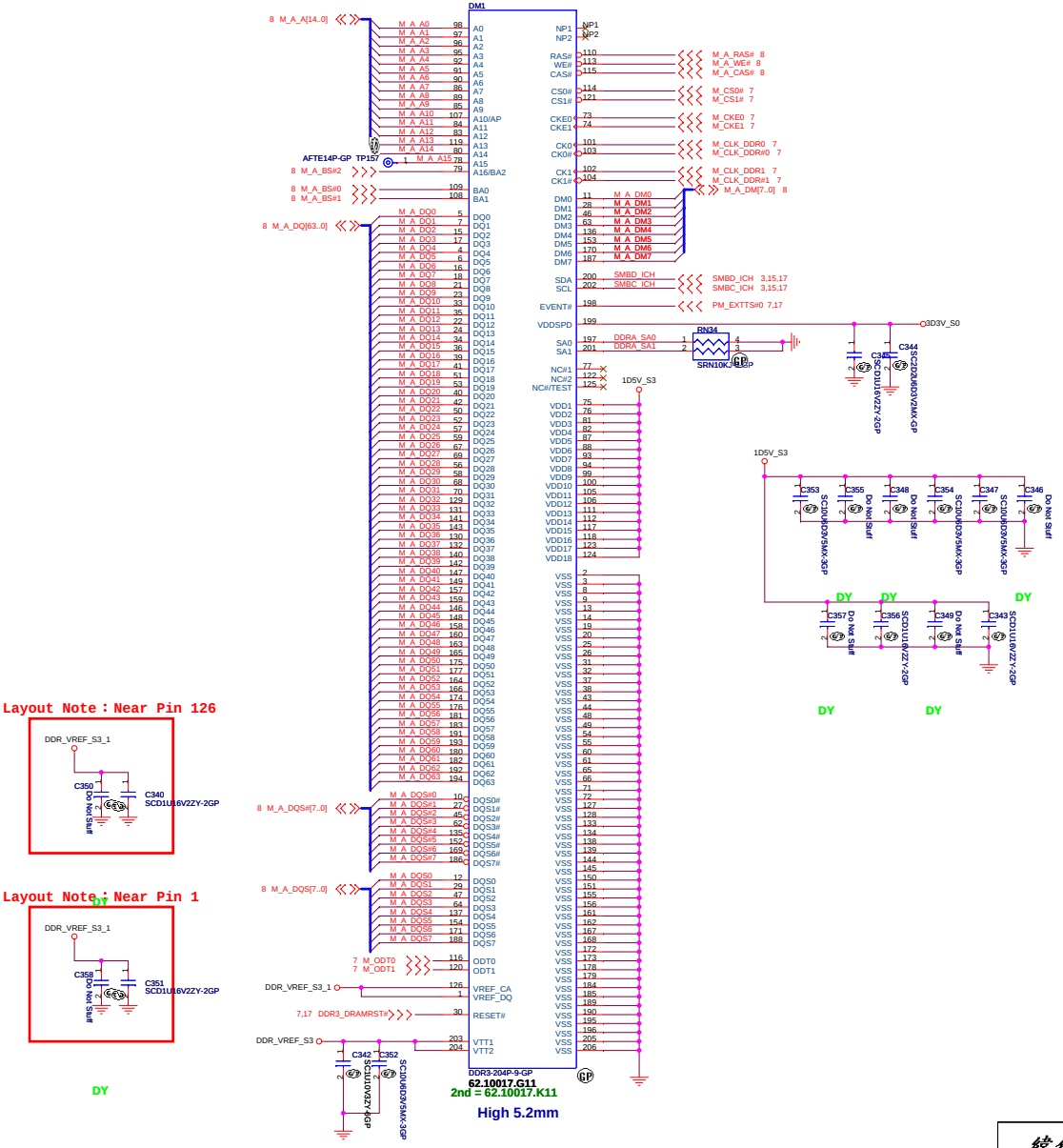
DDR3 SOCKET_1



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR3 Socket
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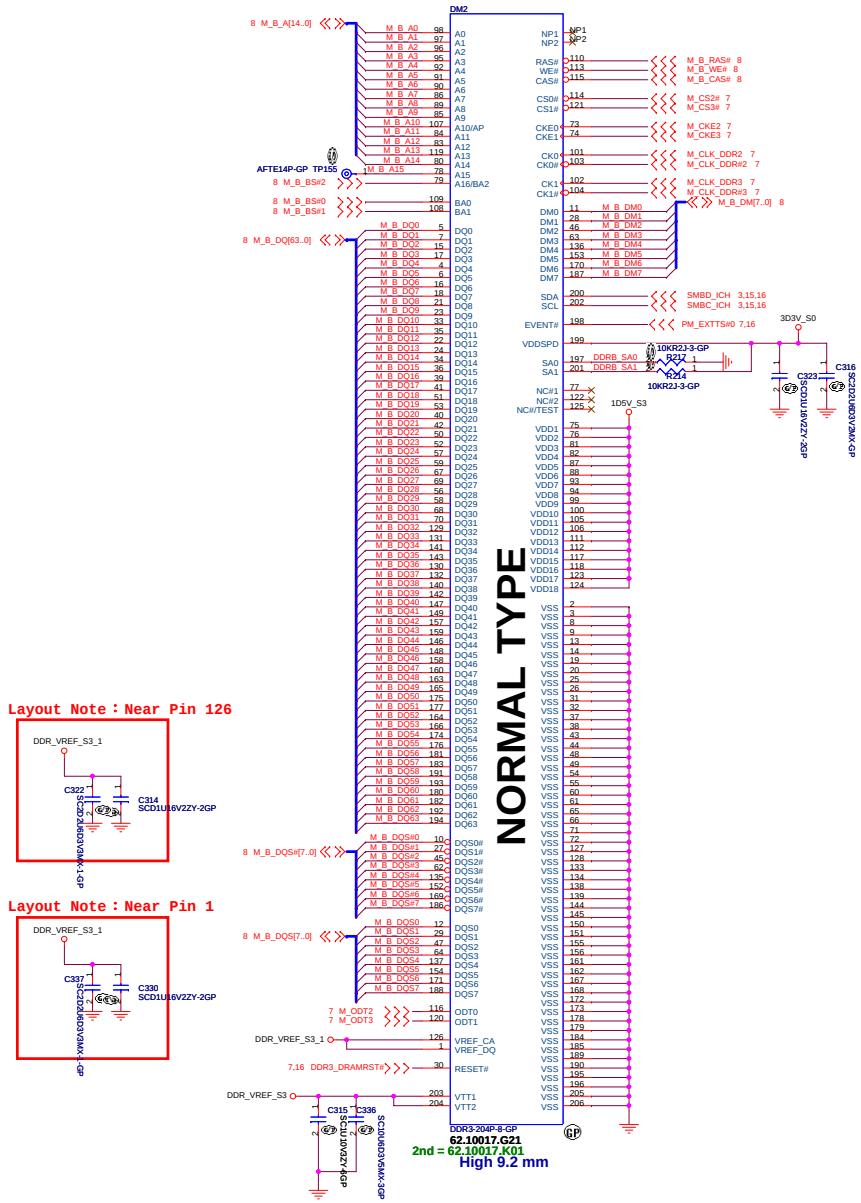
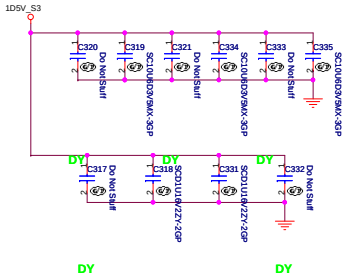
DDR3 SOCKET_2





緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR3 Socket2		
Size	Document Number	Rev	
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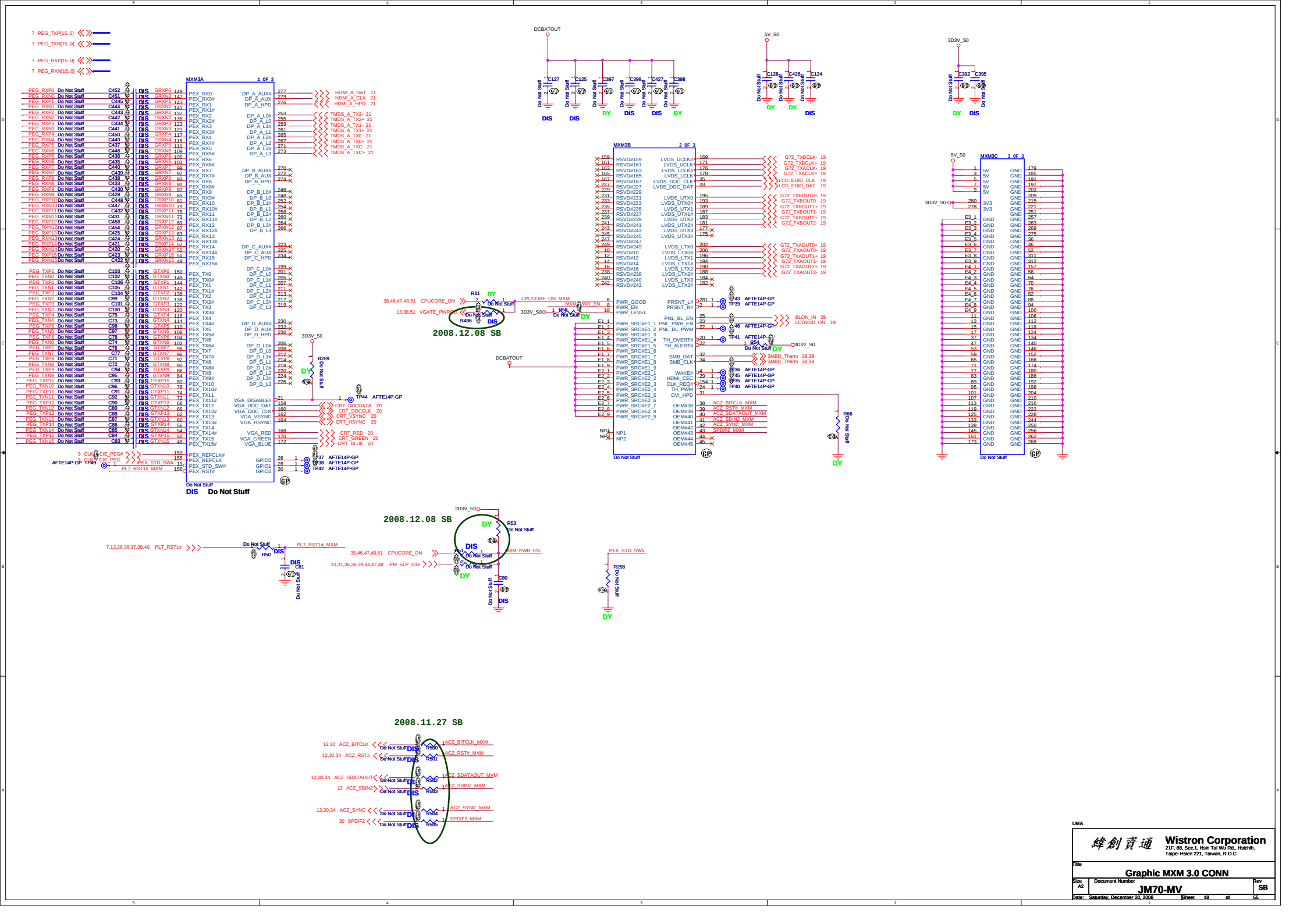
MXM3A
1 OF 3
MXM3B
2 OF 3
MXM3C
3 OF 3
DCBATOUT
5V_S0
3D3V_S0
Do Not Stuff
DIS
DY
2008.12.08 SB
2008.11.27 SB
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM 3.0 CONN
Size A2
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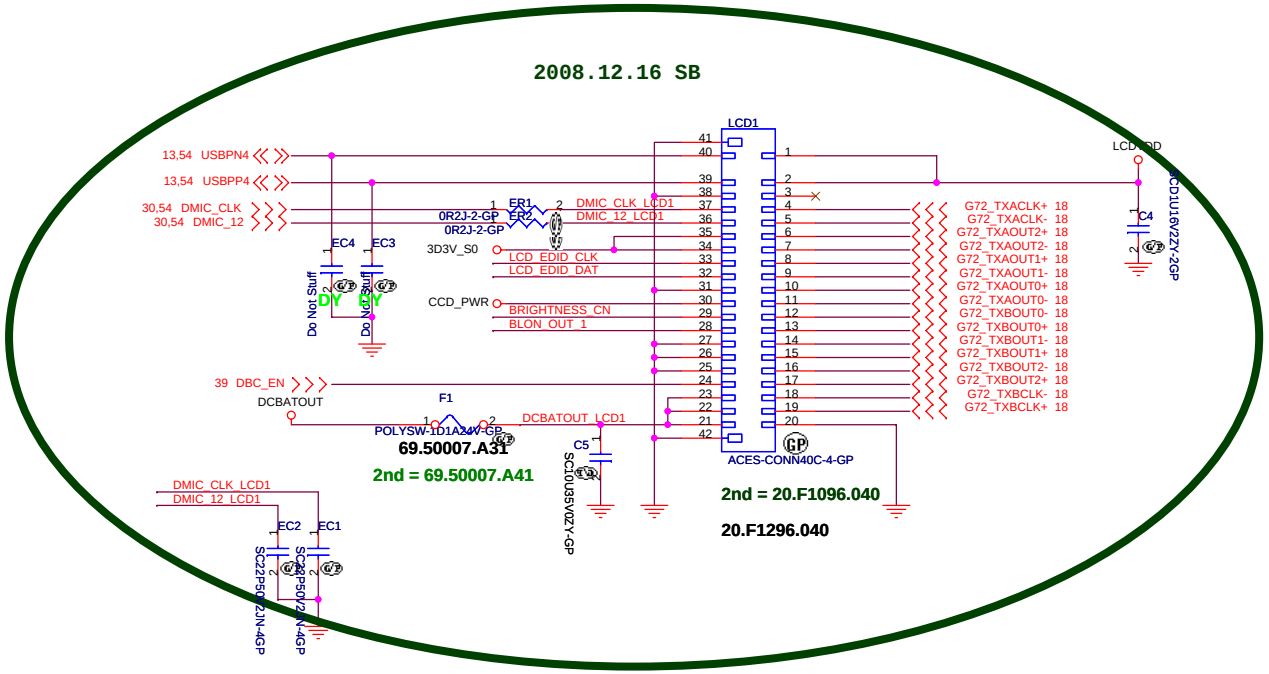
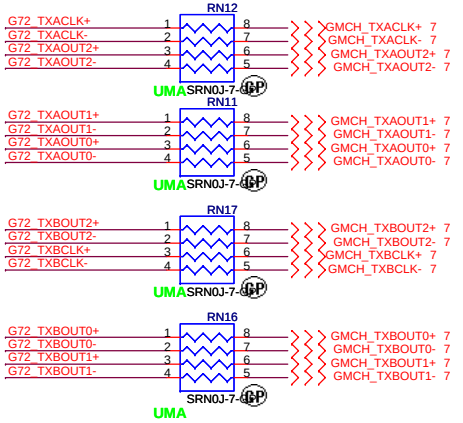
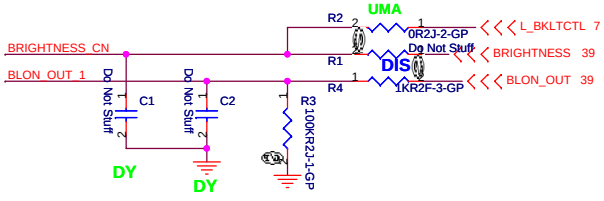
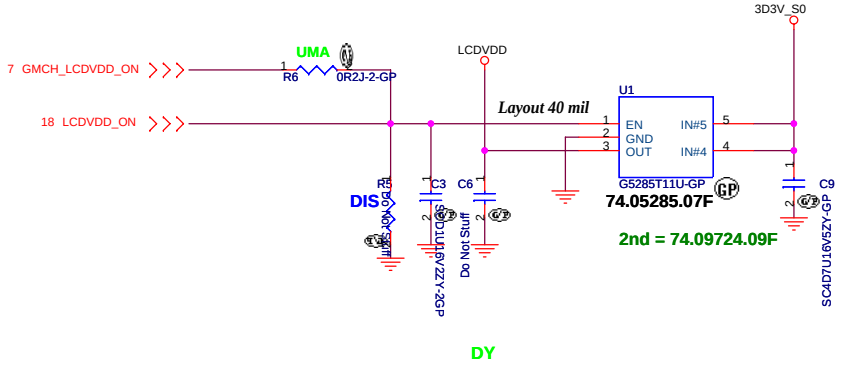
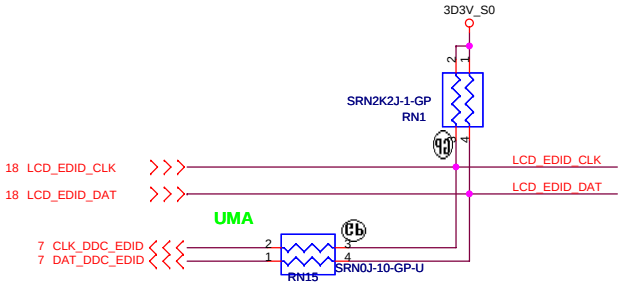
2008.12.16 SB

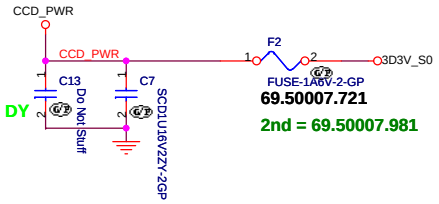












UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LCD CONN**	
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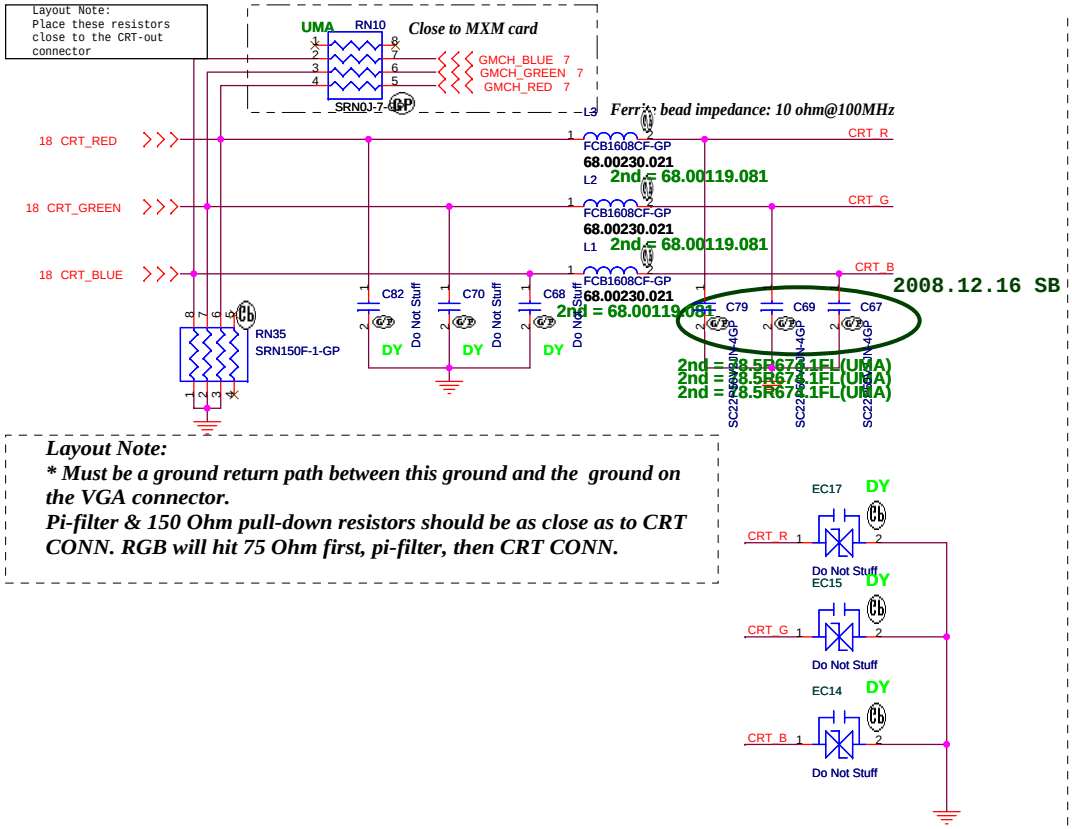

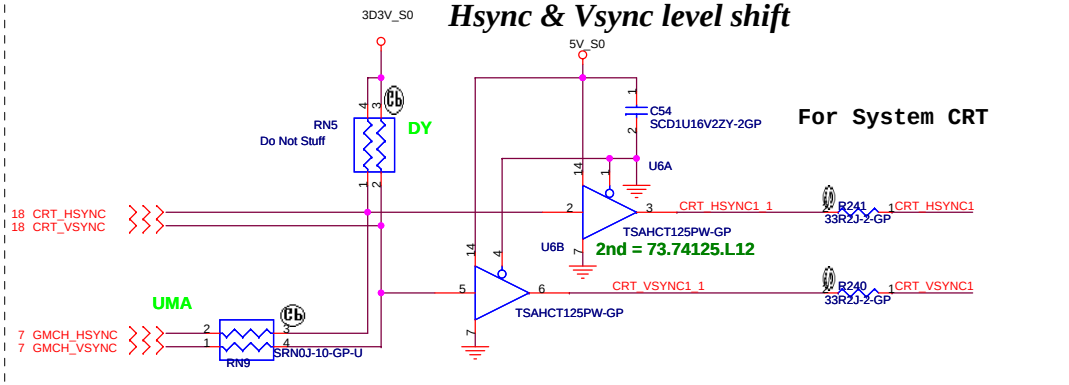

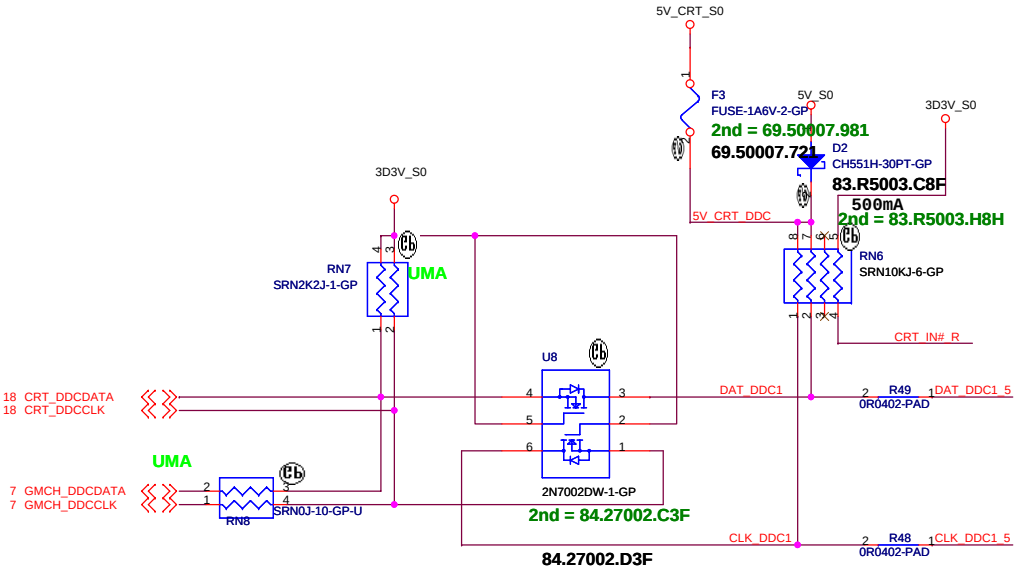

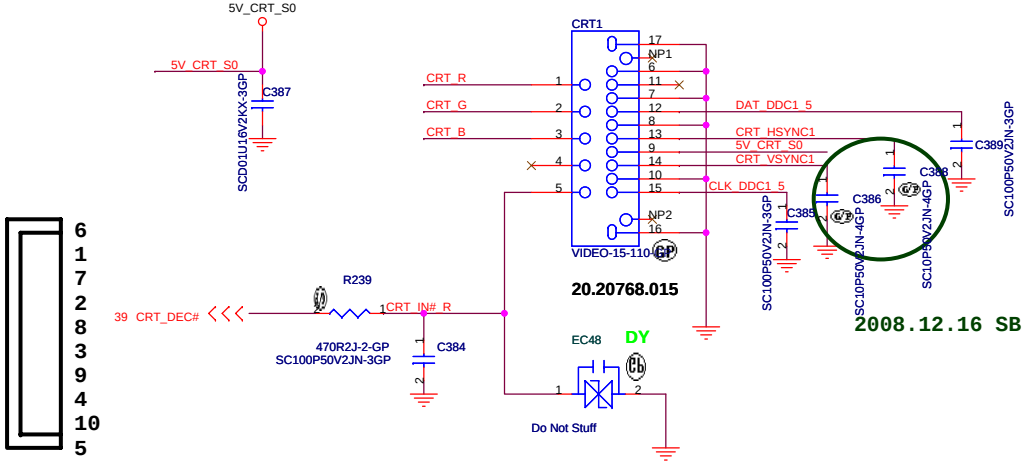

6 1 7 2 8 3 9 4 10 5

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN	
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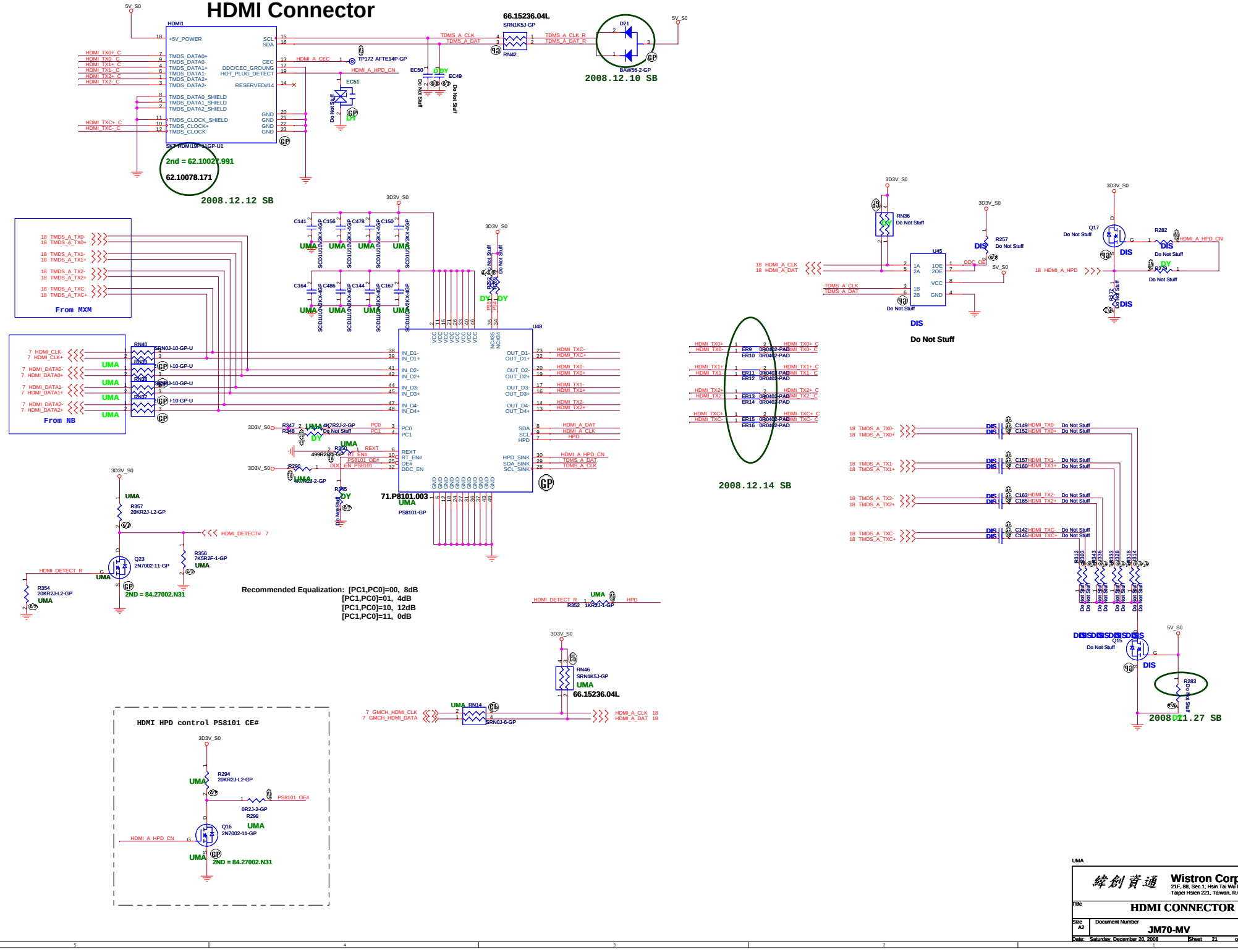
HDMI Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**HDMI CONNECTOR**
Size: A2	Document Number: JM70-MV
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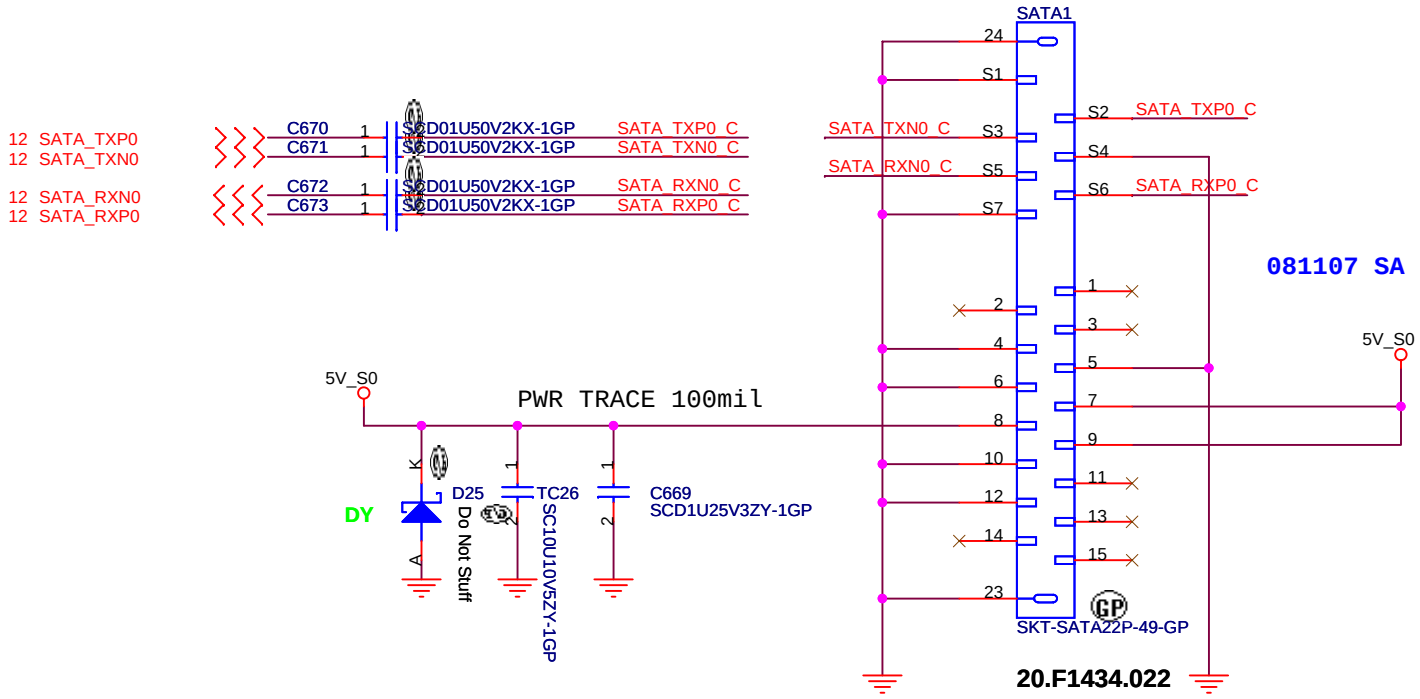
SATA Connector



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD CONN	
Size	Document Number: JM70-MV	Rev: SB
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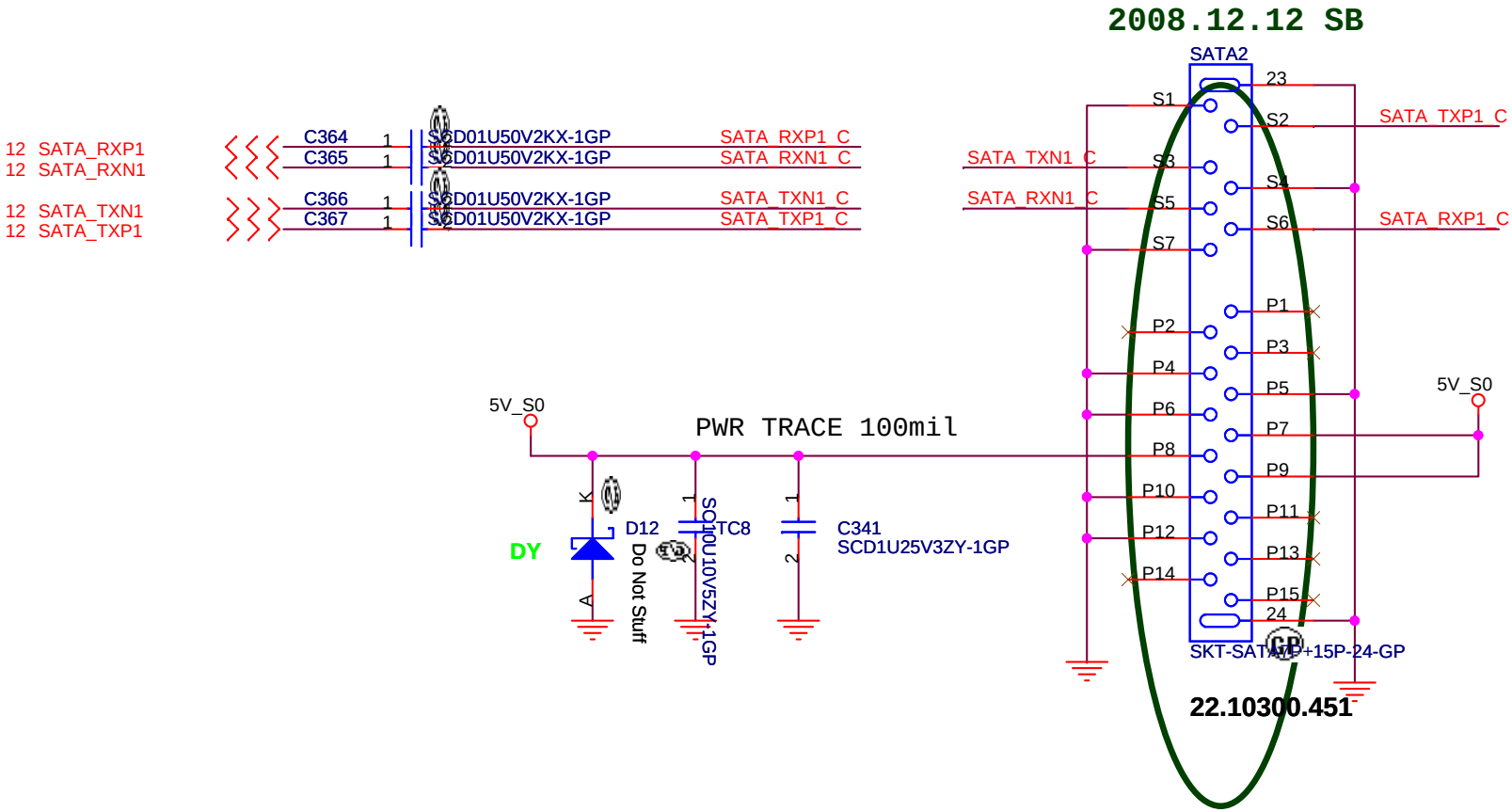
2nd HDD SATA Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***2nd HDD***		
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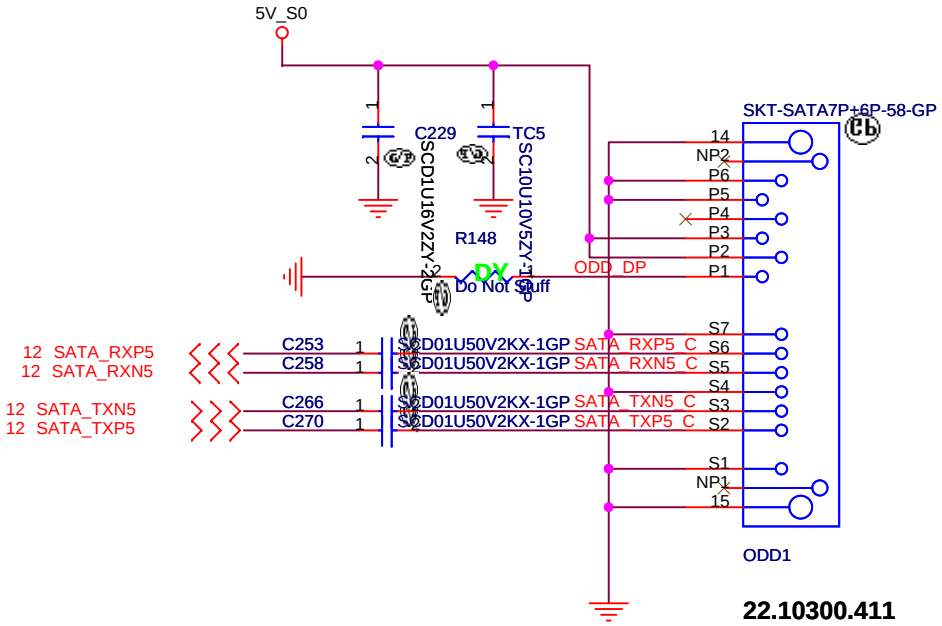
ODD Connector



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***ODD***	
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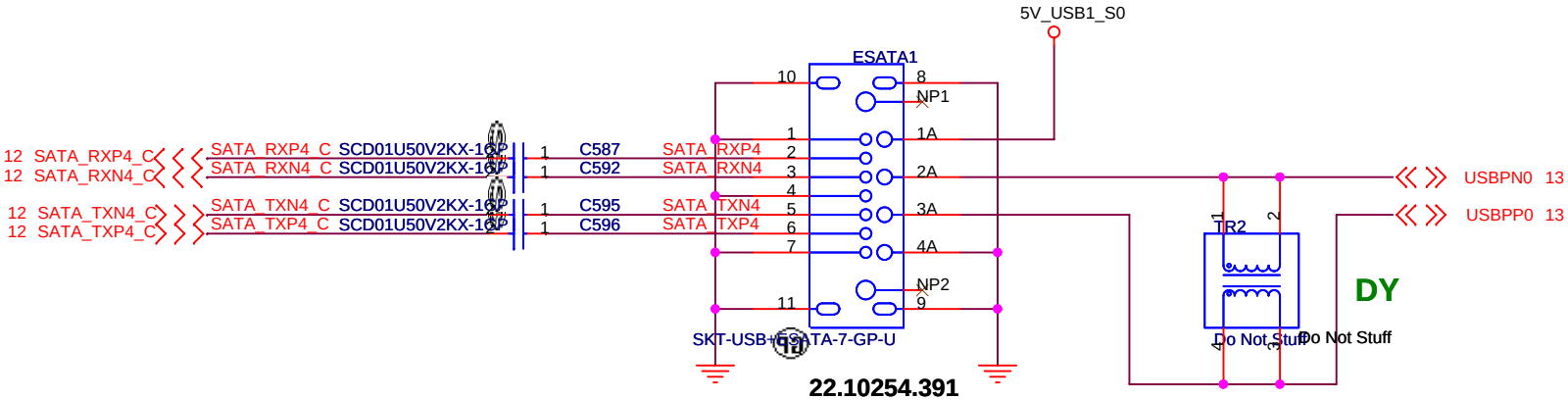
ESATA Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ESATA*		
Size: A4	Document Number: JM70-MV	Rev: SB
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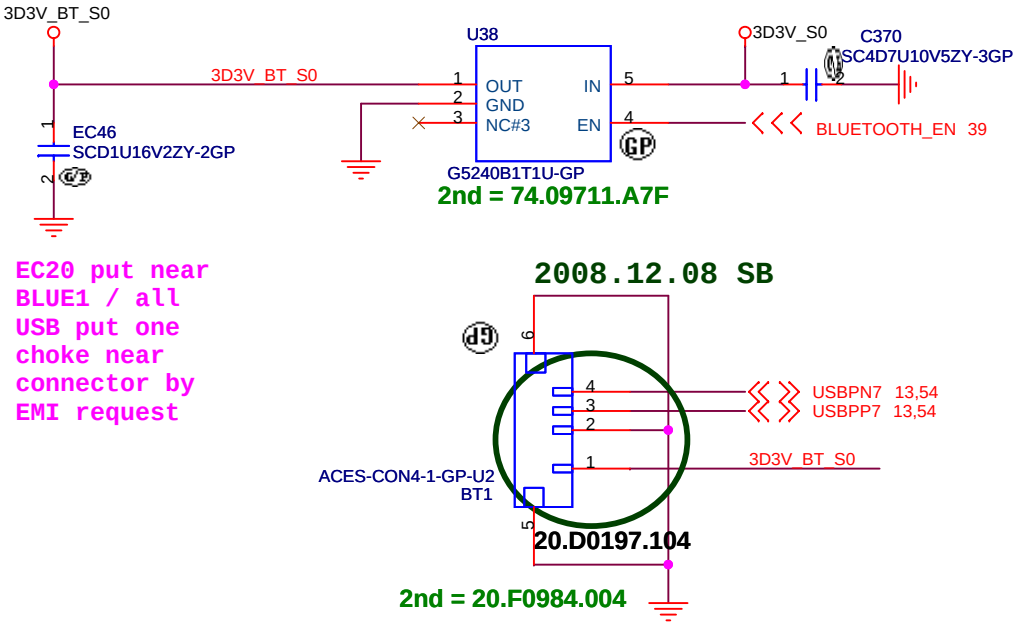
BLUETOOTH MODULE



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
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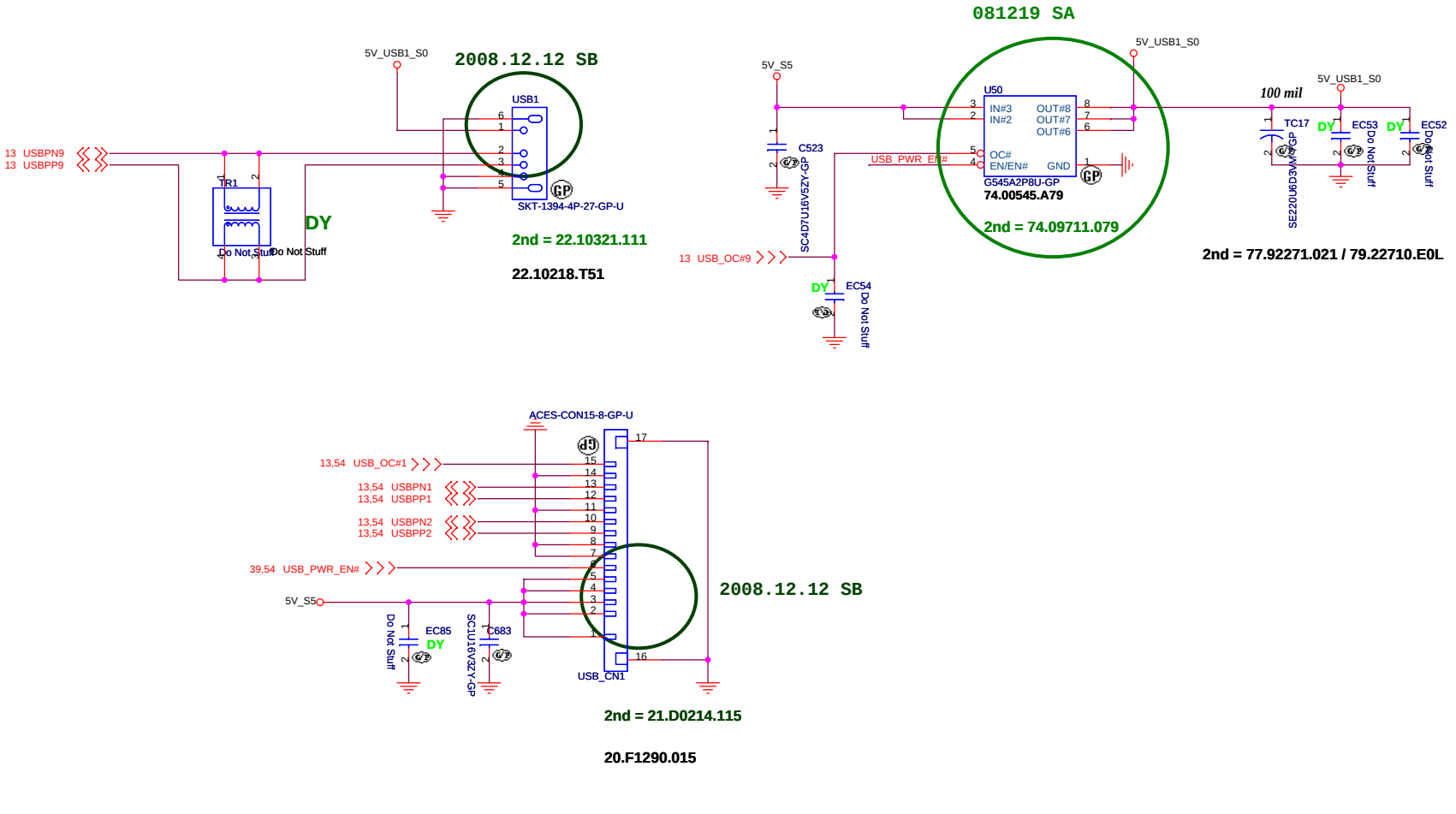
USB1 Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB CONN*		
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2008.12.14 SB

72.24C64.F01

Place PLLVDD/AVDDL CKT as close to chip as possible

2008.12.14 SB

2008.12.08 SB

R349 change to Bead for Transmitter Distortion

2nd = 82.30020.851

2nd = 71.05784.M03

2nd = 68.00248.011

2nd = 84.DCP69.01B

UMA		
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BCM5764	
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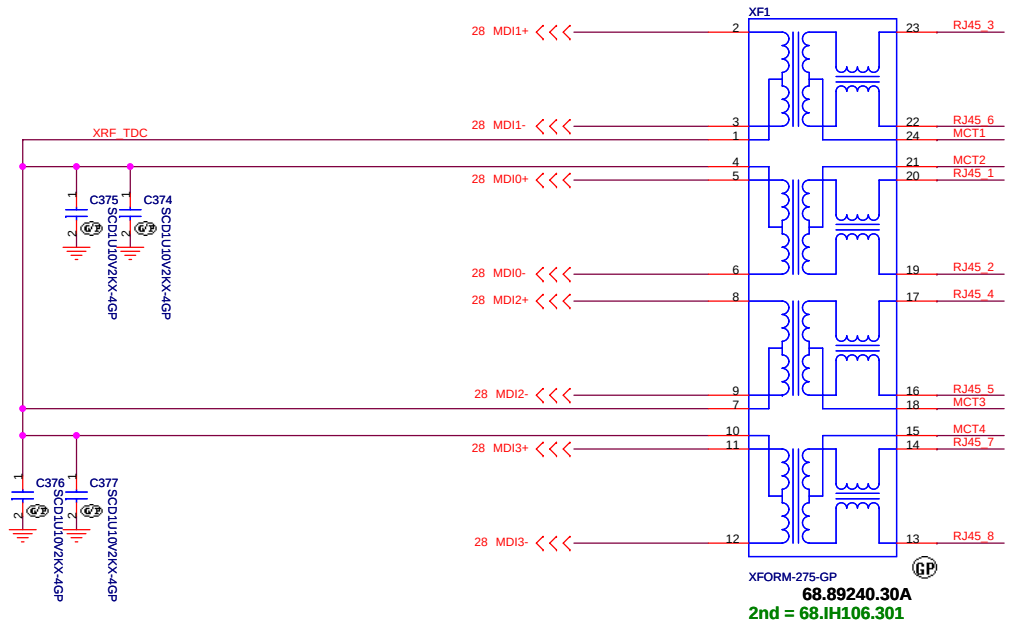
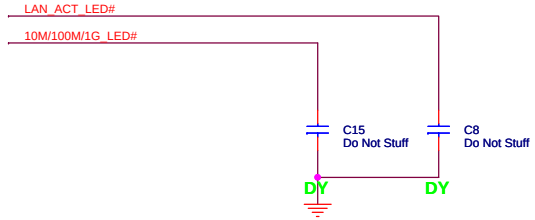
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

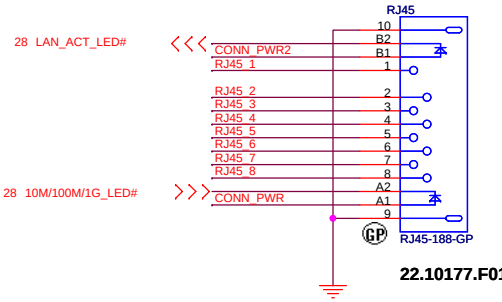
LAN Connector

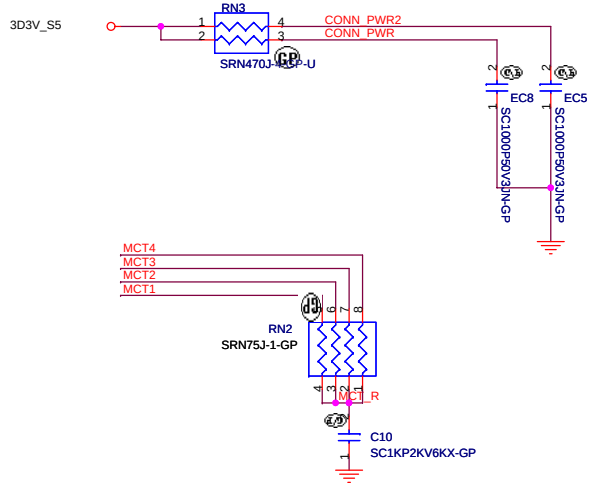
LAN Connector

GIGA Lan Transformer









UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JM70-MV	Rev: SB
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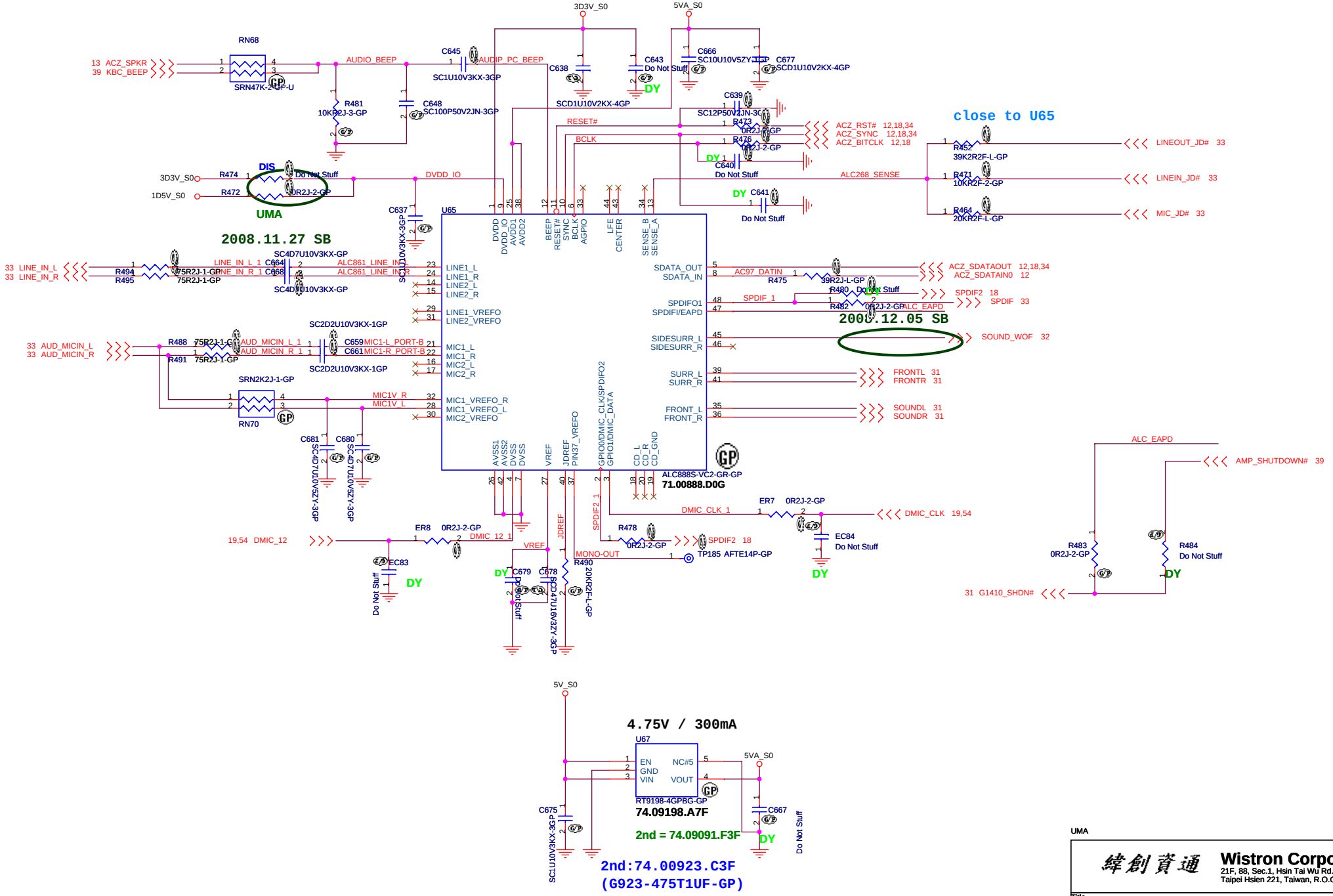

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC888***

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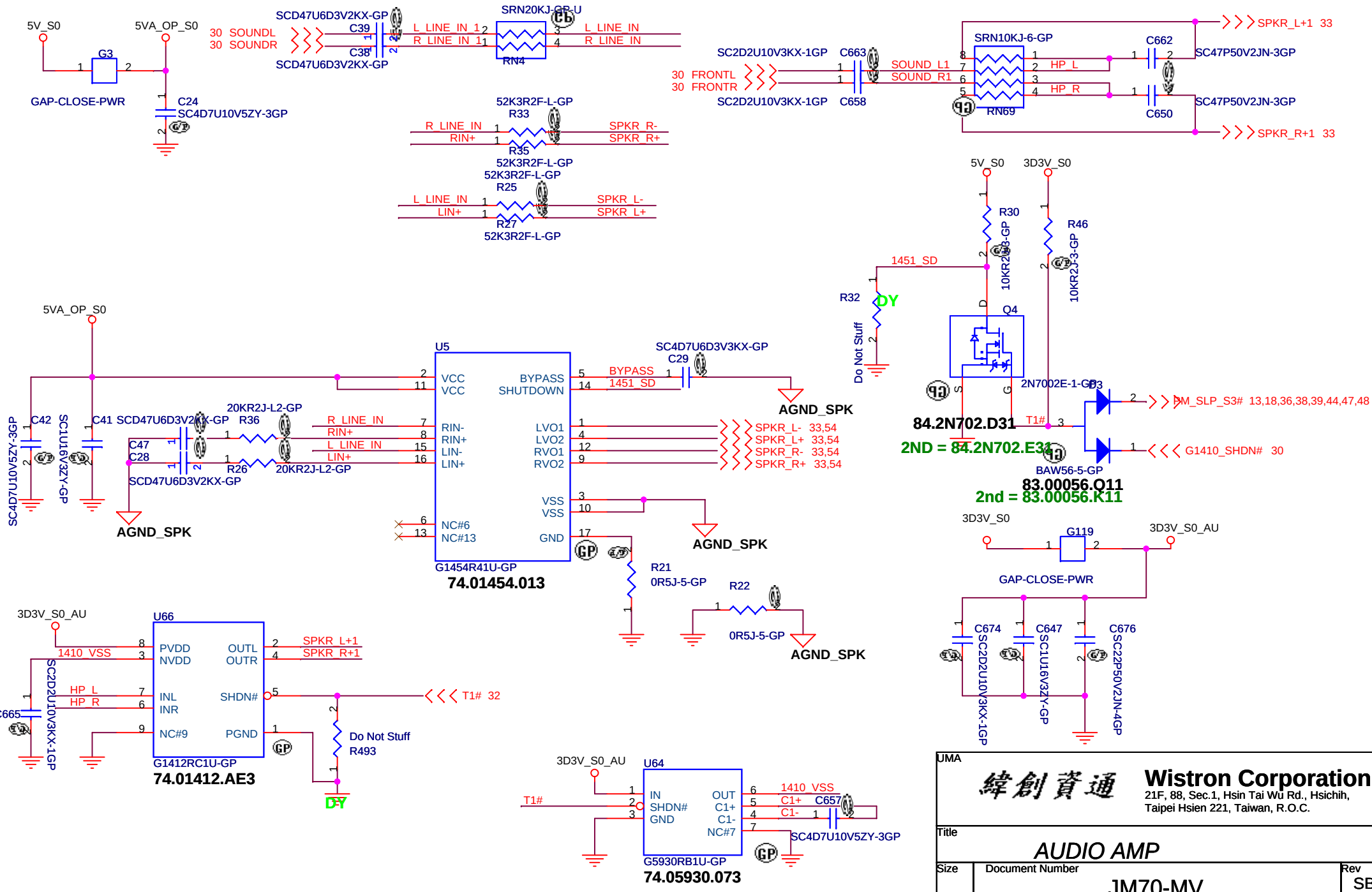
AUDIO OP AMPLIFIER



UMA	緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO AMP*	
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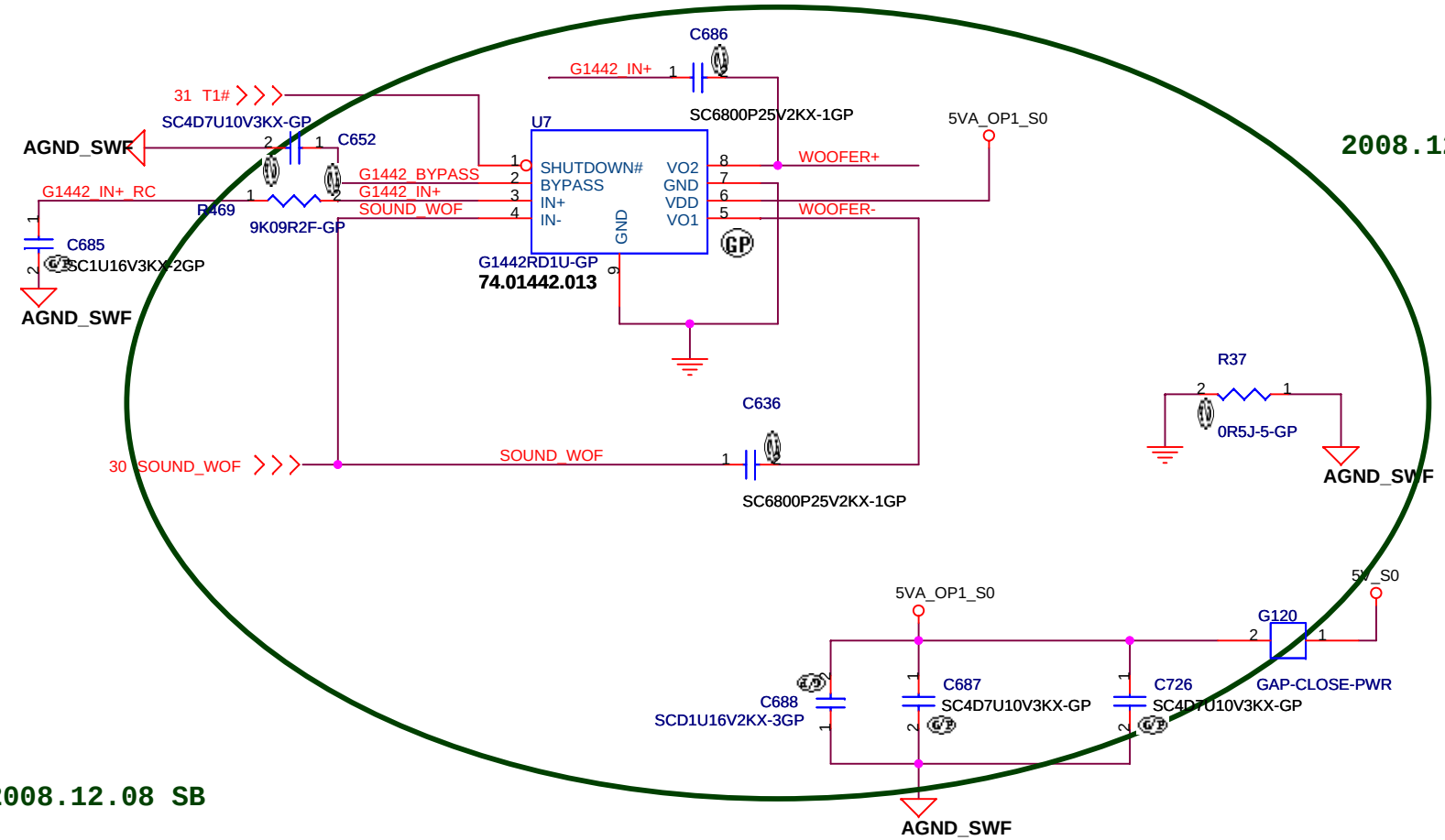

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SUBWOOFER CONN.***

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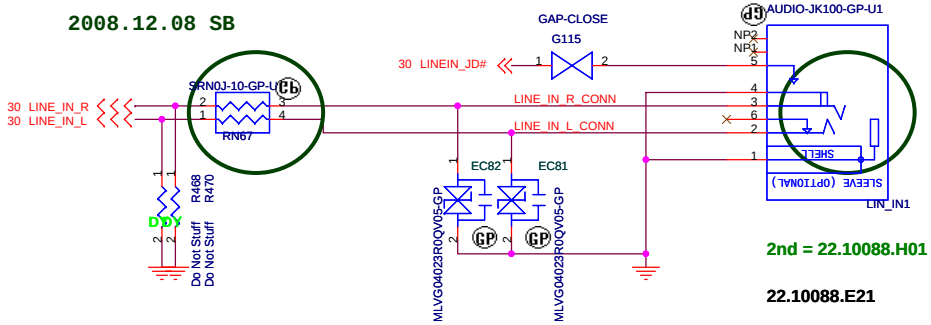
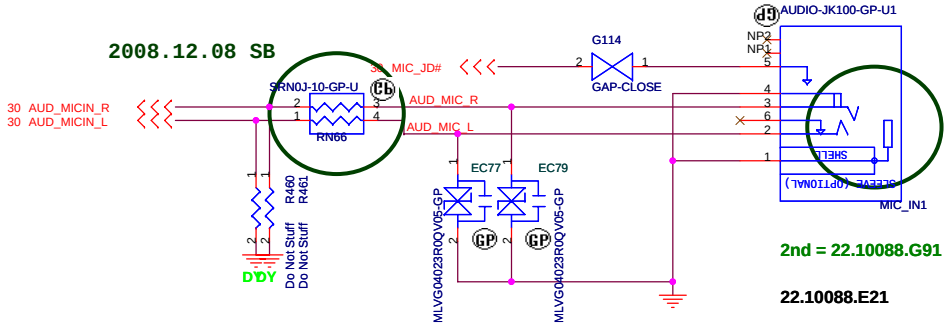
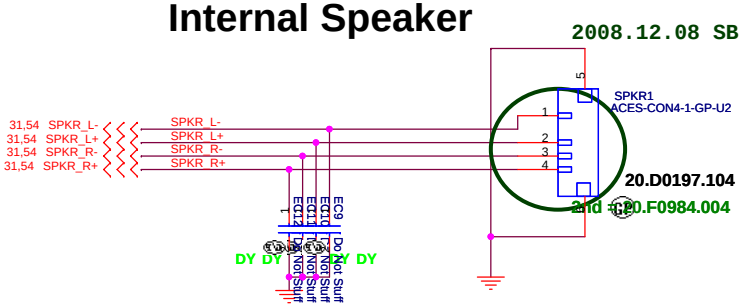
LINE IN



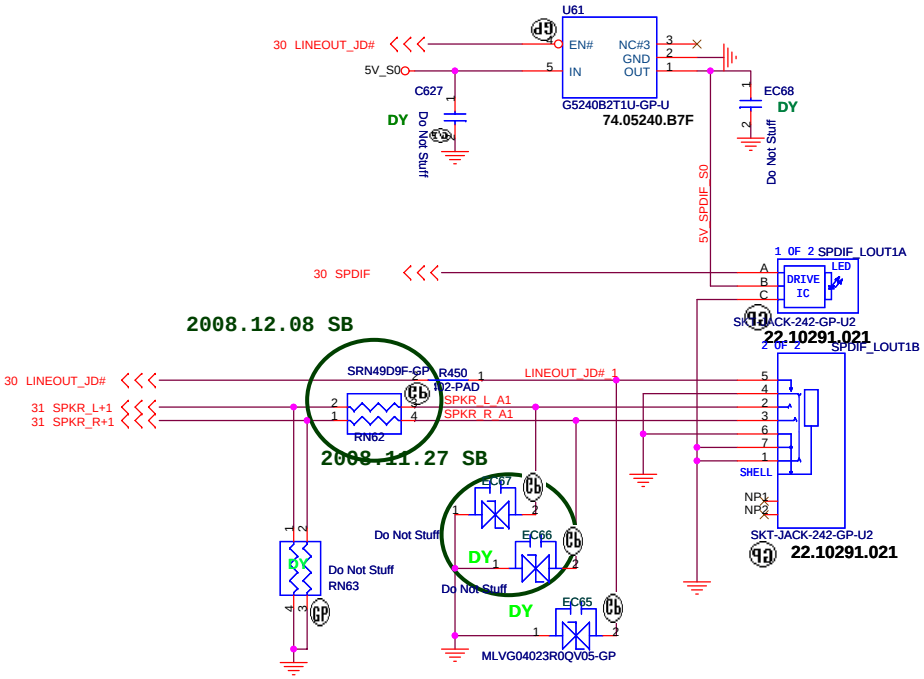
MIC IN



Internal Speaker



LINE OUT / SPDIF



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO jack*		
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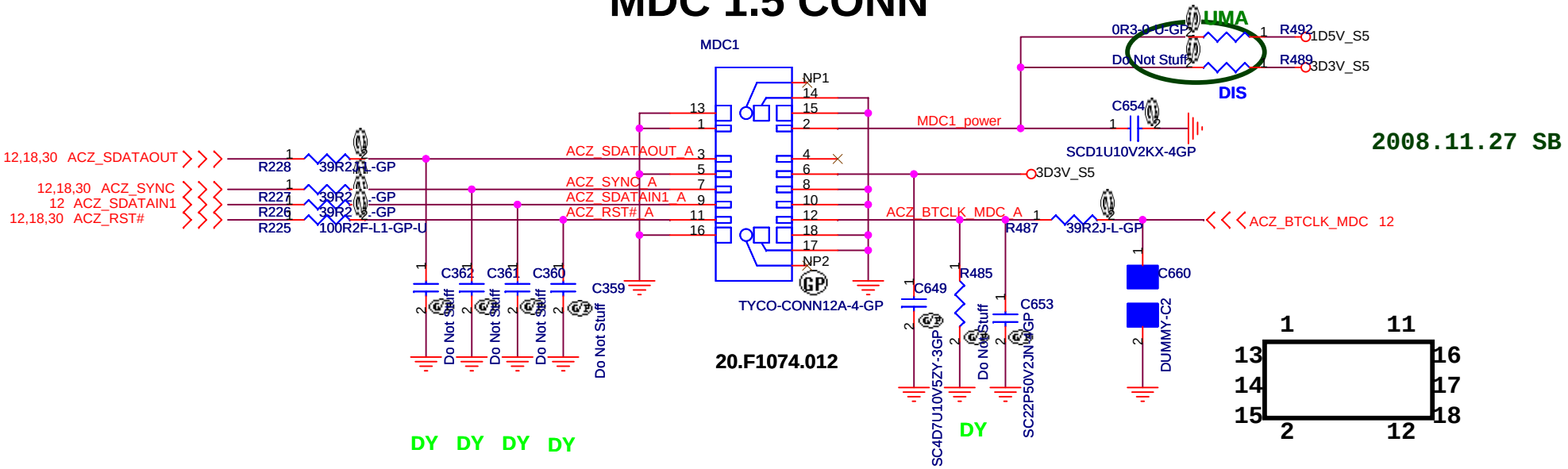
MDC 1.5 CONN



2008.11.27 SB

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
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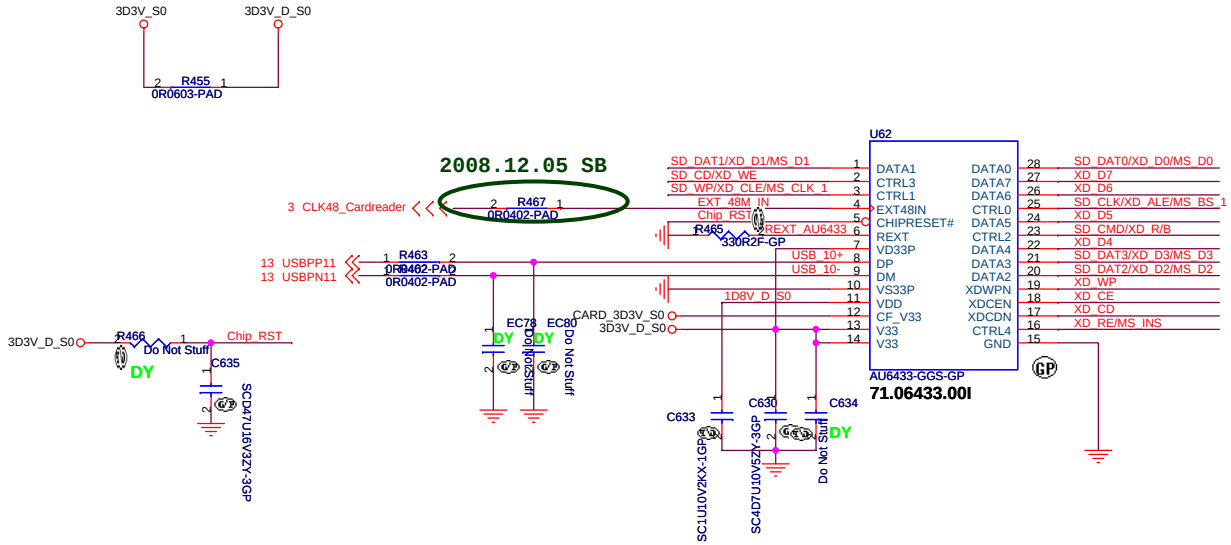
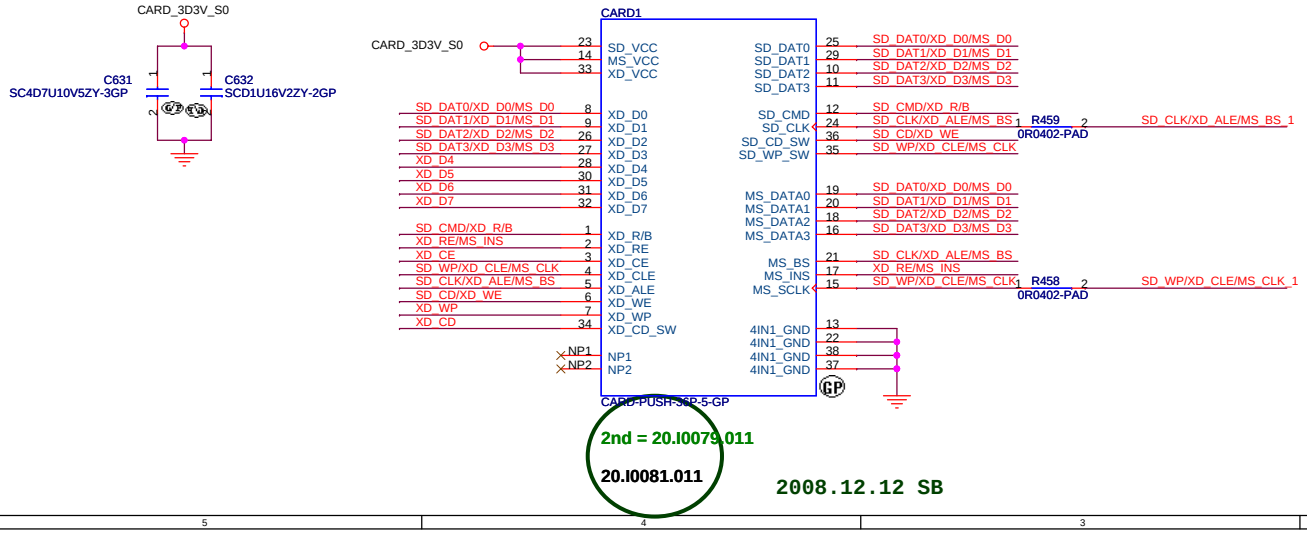
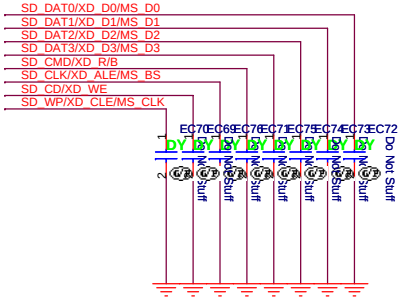


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



EMI capacitor



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader*	
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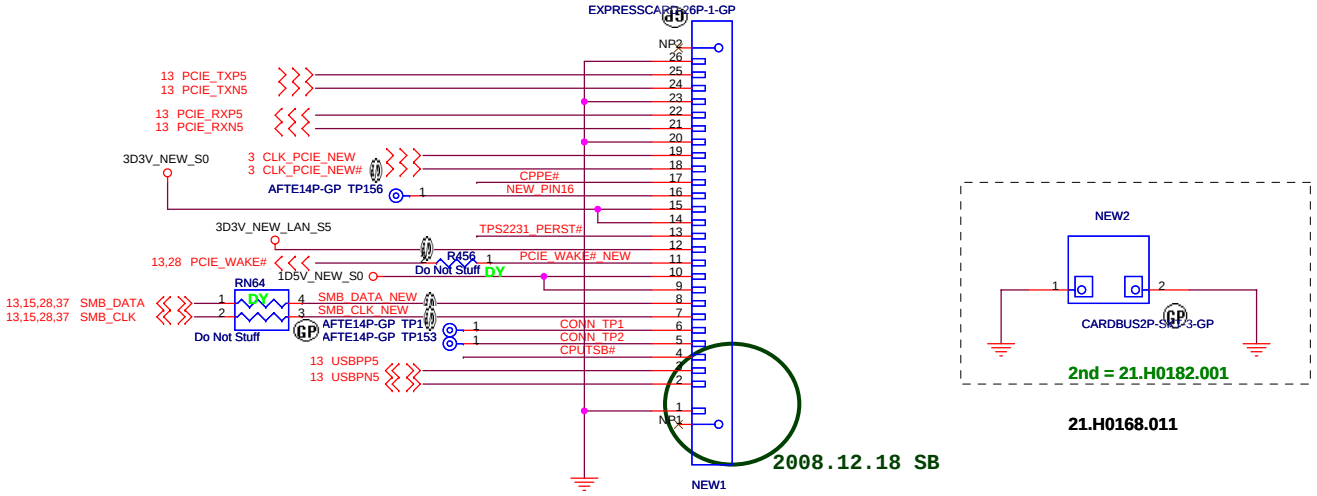
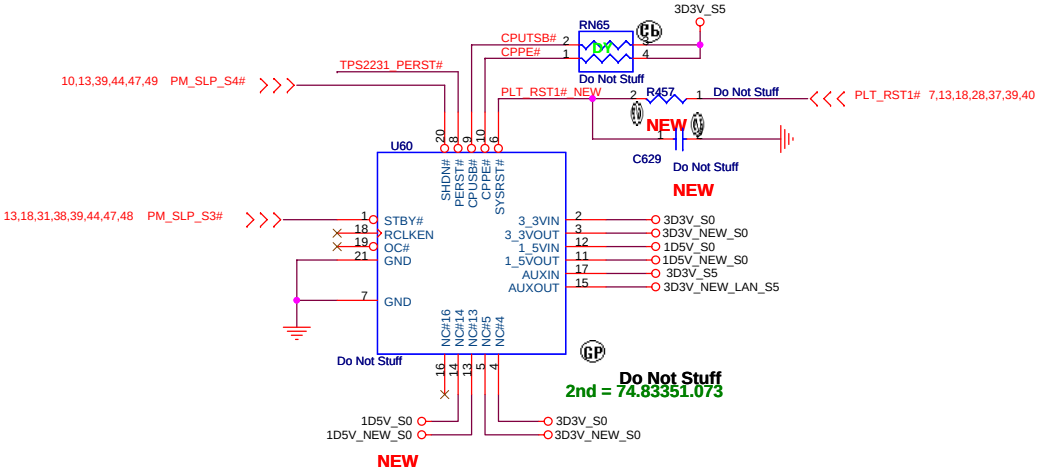
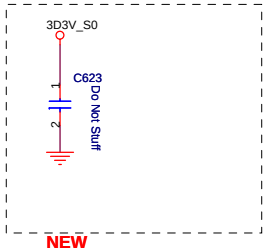
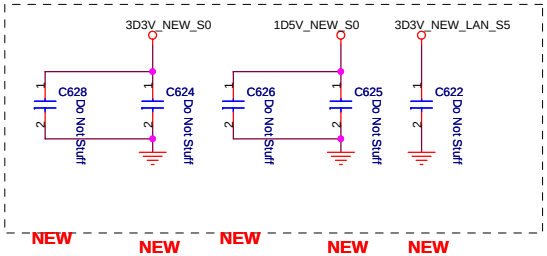




Place them Near to Chip



Place them Near to Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***NEW CARD***	
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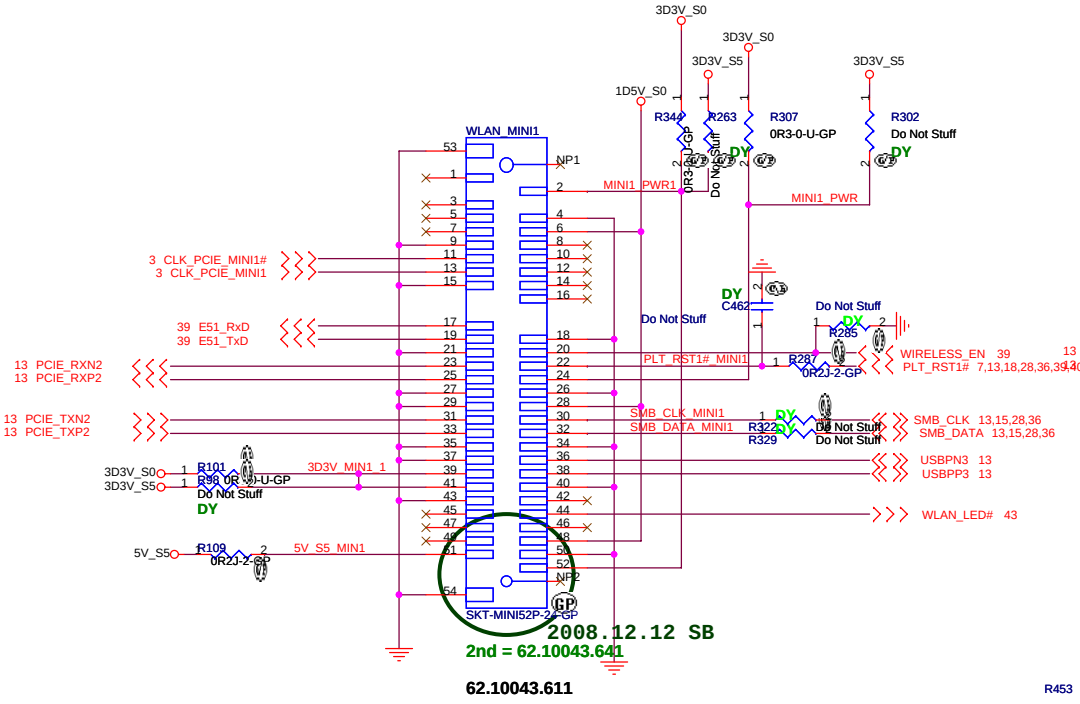
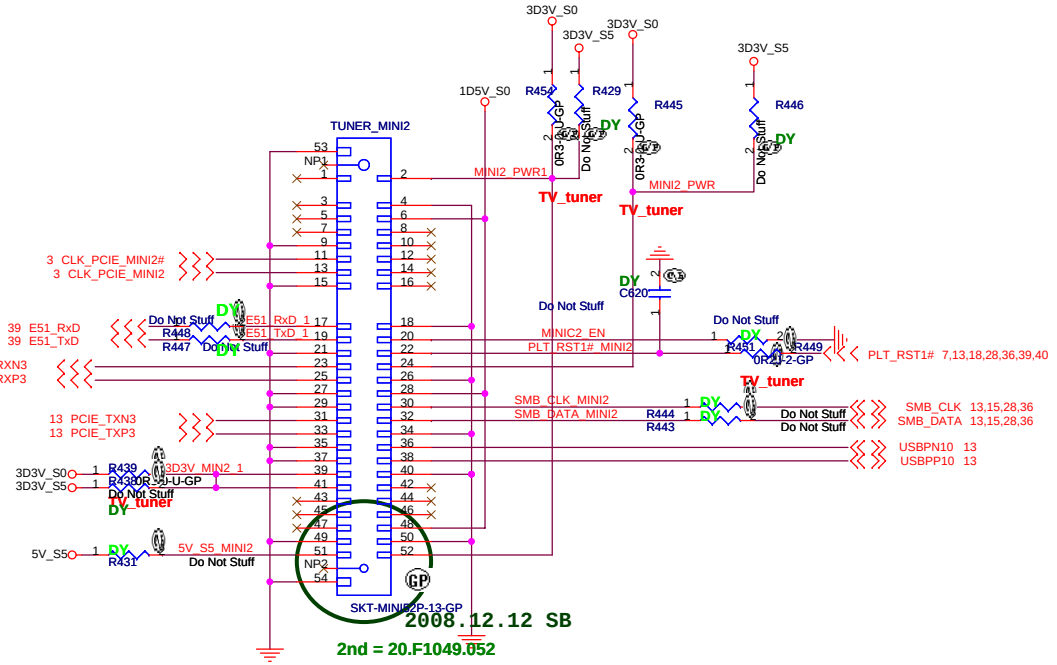
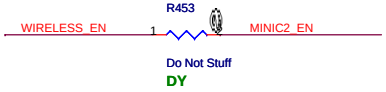
Mini1 Card Connector(WLAN)
Support debug-card

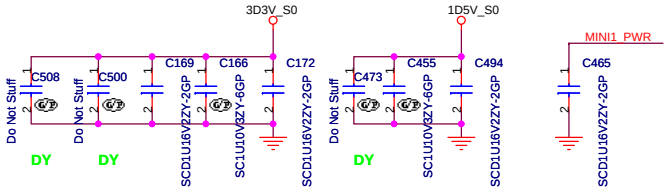


Mini2 Card Connector(TV tuner)

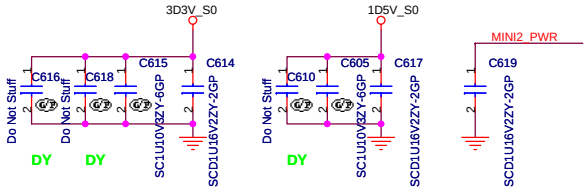




Place near MINI1



Place near MINIC2



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: JM70-MV	Rev: SB
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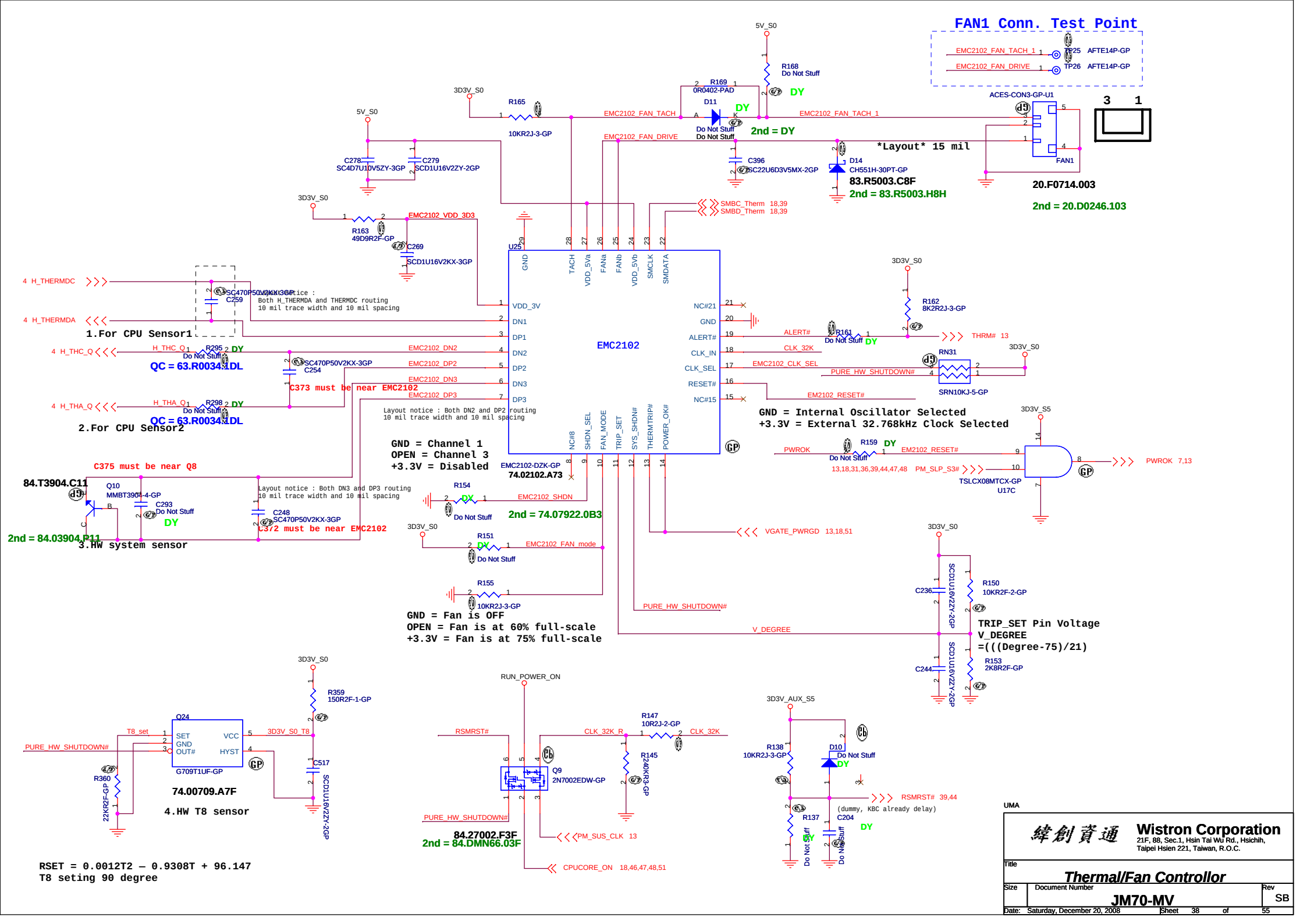
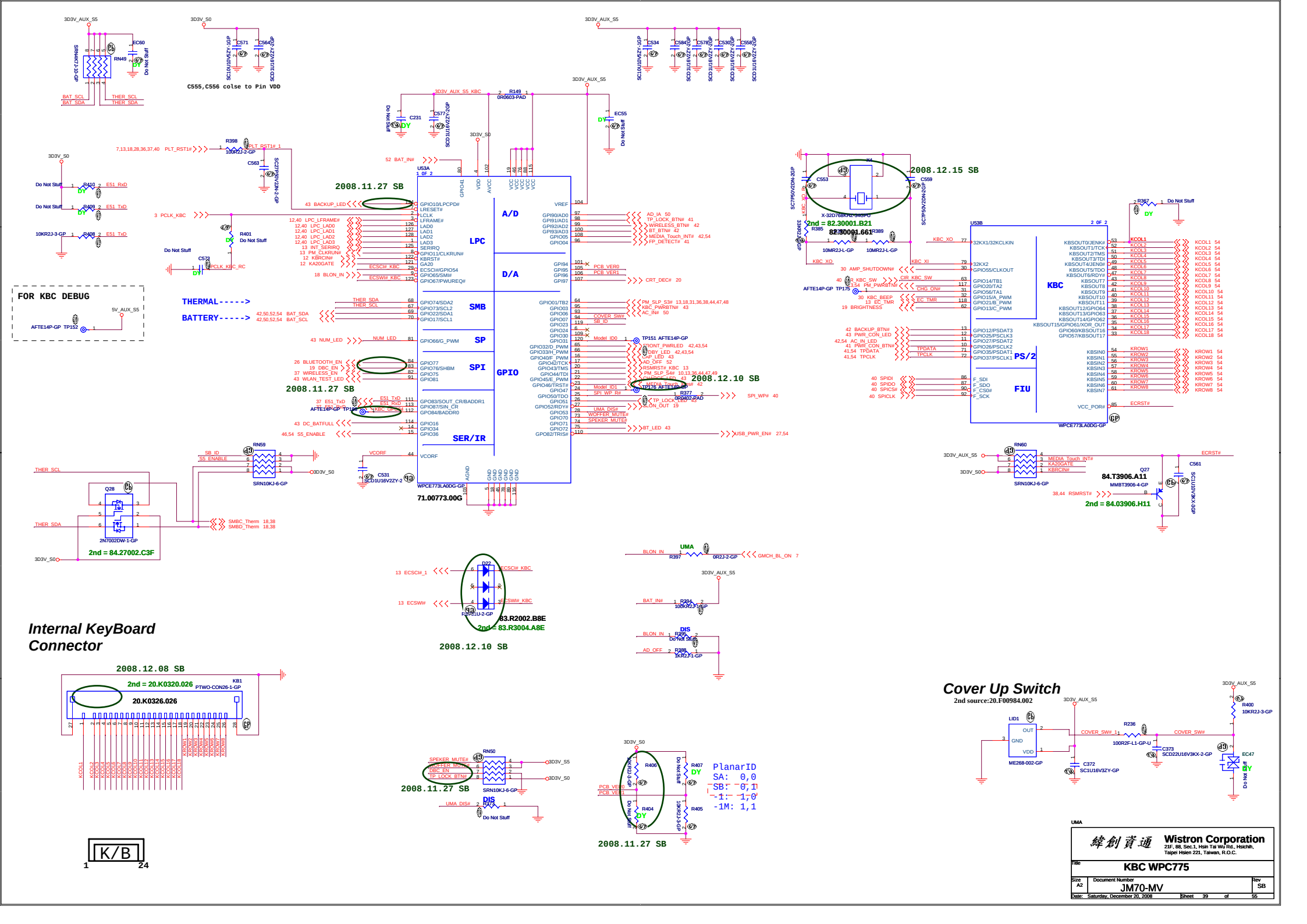
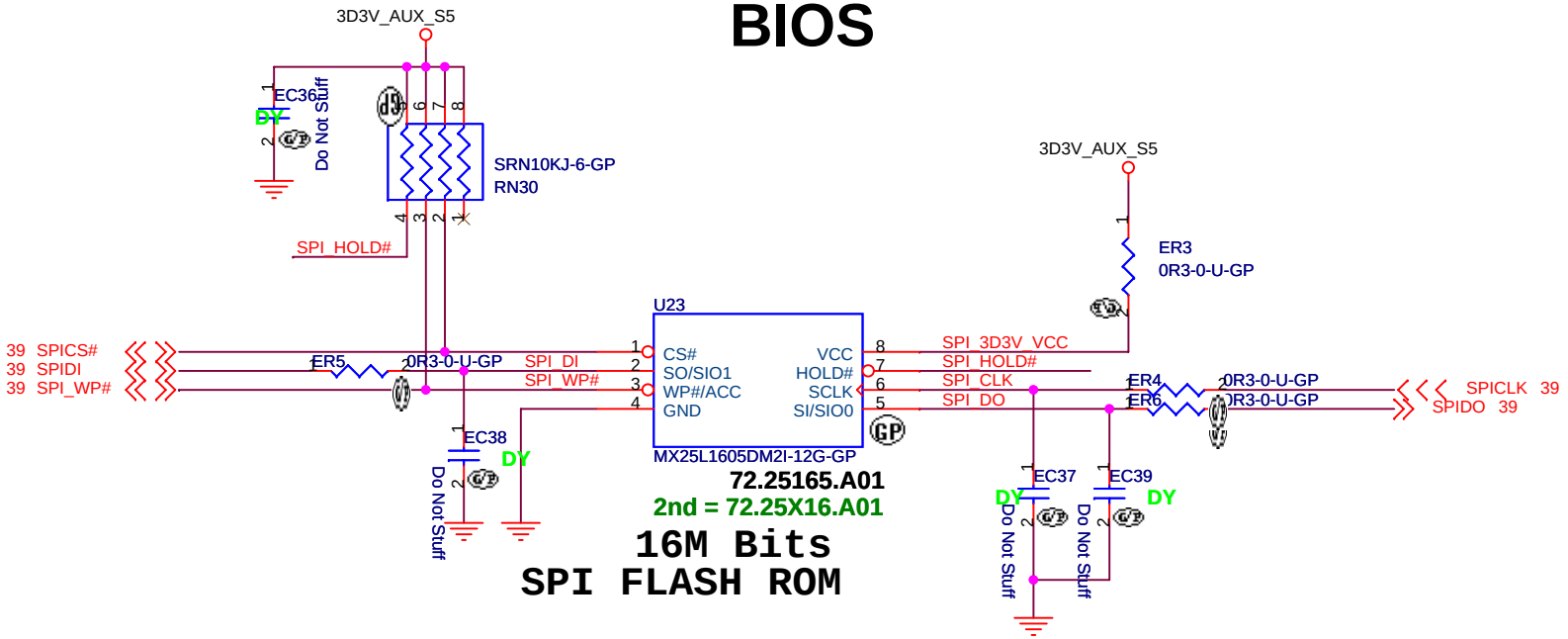
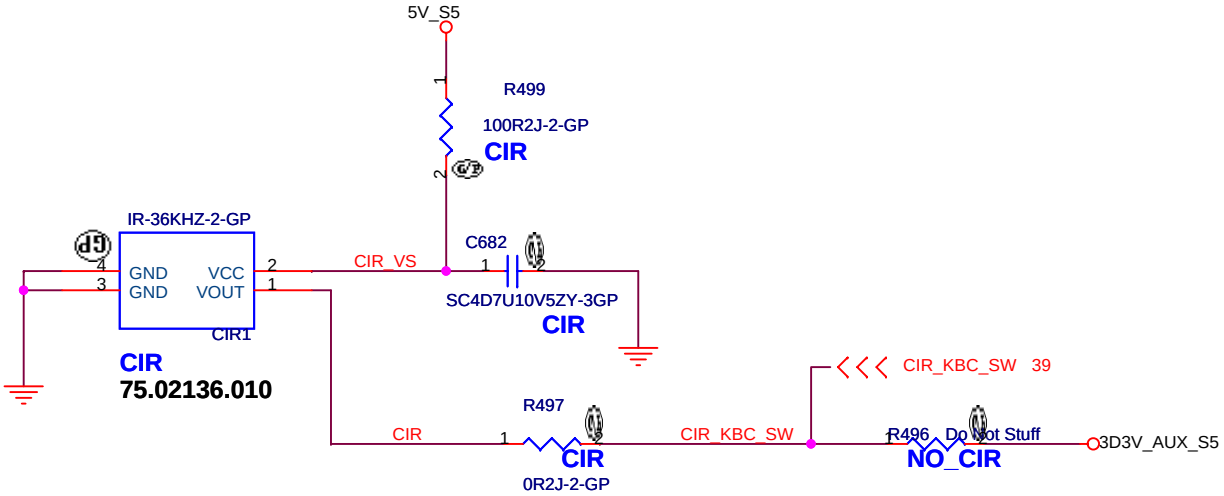

FAN1 Conn. Test Point
EMC2102_FAN_TACH_1
TP25 AFTE14P-GP
EMC2102_FAN_DRIVE
TP26 AFTE14P-GP
ACES-CON3-GP-U1
FAN1
Layout 15 mil
83.R5003.C8F
2nd = 83.R5003.H8H
20.F0714.003
2nd = 20.D0246.103
EMC2102
EMC2102-DZK-GP
74.02102.A73
1.For CPU Sensor1
2.For CPU Sensor2
3.HW system sensor
4.HW T8 sensor
QC = 63.R0034.1DL
C373 must be near EMC2102
C372 must be near EMC2102
C375 must be near Q8
84.T3904.C11
2nd = 84.03904.P11
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
2nd = 74.07922.0B3
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
74.00709.A7F
84.27002.F3F
2nd = 84.DMN66.03F
RSET = 0.0012T2 – 0.9308T + 96.147
T8 seting 90 degree
Layout notice : Both H_THERMDA and THERMDC routing 10 mil trace width and 10 mil spacing
Layout notice : Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing
Layout notice : Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thermal/Fan Controllor
JM70-MV
Saturday, December 20, 2008
Sheet 38 of 55


3D3V_AUX_S5
3D3V_S0
C555,C556 colse to Pin VDD
2008.11.27 SB
2008.12.15 SB
2008.12.10 SB
2008.12.08 SB
2008.11.27 SB
2008.12.10 SB
2008.11.27 SB
U53A
WPCE773LA0DG-GP
71.00773.00G
KBC
PS/2
FIU
X4
X-32D768KHZ-3GPD
2nd = 82.30001.B21
82.30001.661
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
KB1
PTWO-CON26-1-GP
20.K0326.026
2nd = 20.K0320.026
2N7002DW-1-GP
2nd = 84.27002.C3F
SRN10KJ-6-GP
2nd = 84.03906.H11
MMBT3906-4-GP
84.T3906.A11
ME268-002-GP
Cover Up Switch
2nd source:20.F00984.002
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
K/B
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JM70-MV
Saturday, December 20, 2008

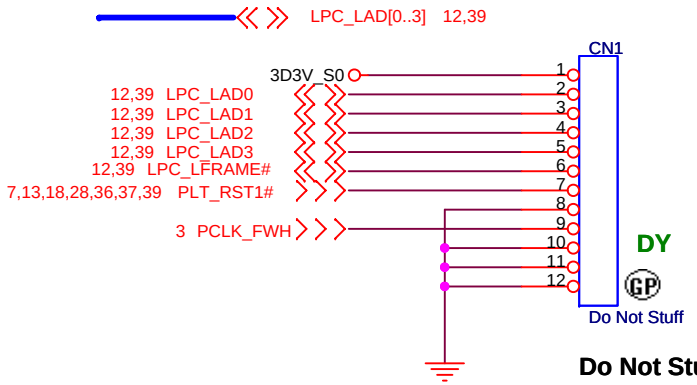
BIOS



VISHAY CIR Module



GOLDEN FINGER FOR DEBUG BOARD



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
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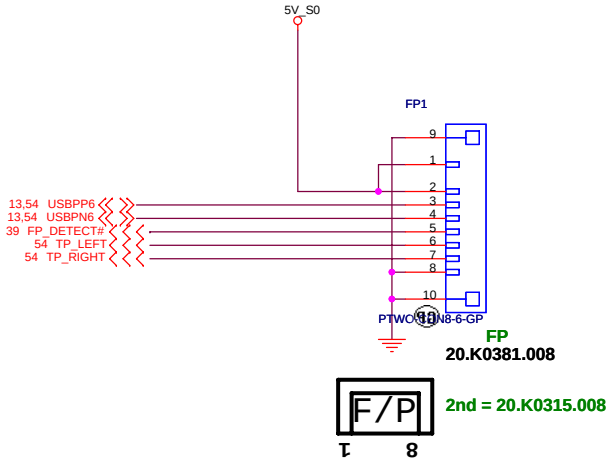
Date: Saturday, December 20, 2008	Sheet 40 of 55	

Finger printer



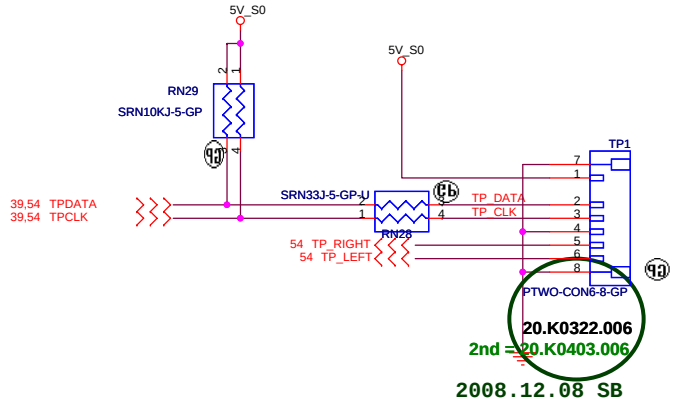
FP

20.K0381.008

F/P

2nd = 20.K0315.008

Touch Pad

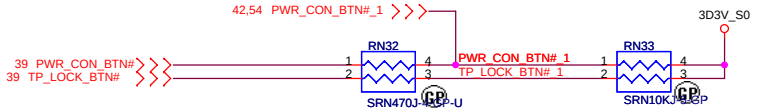


20.K0322.006

2nd = 20.K0403.006

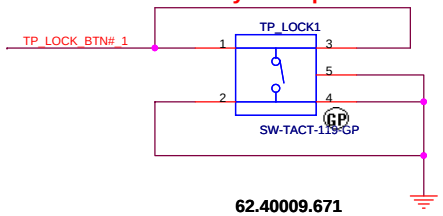
2008.12.08 SB

T/P



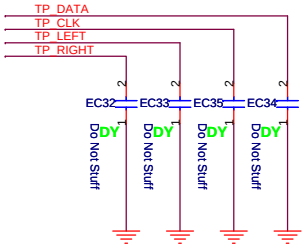
TP_LOCK key

Note. main with 2nd symbol pin define different



62.40009.671

2nd = 62.40012.101



UMA

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD and FP		
Size	Document Number	Rev
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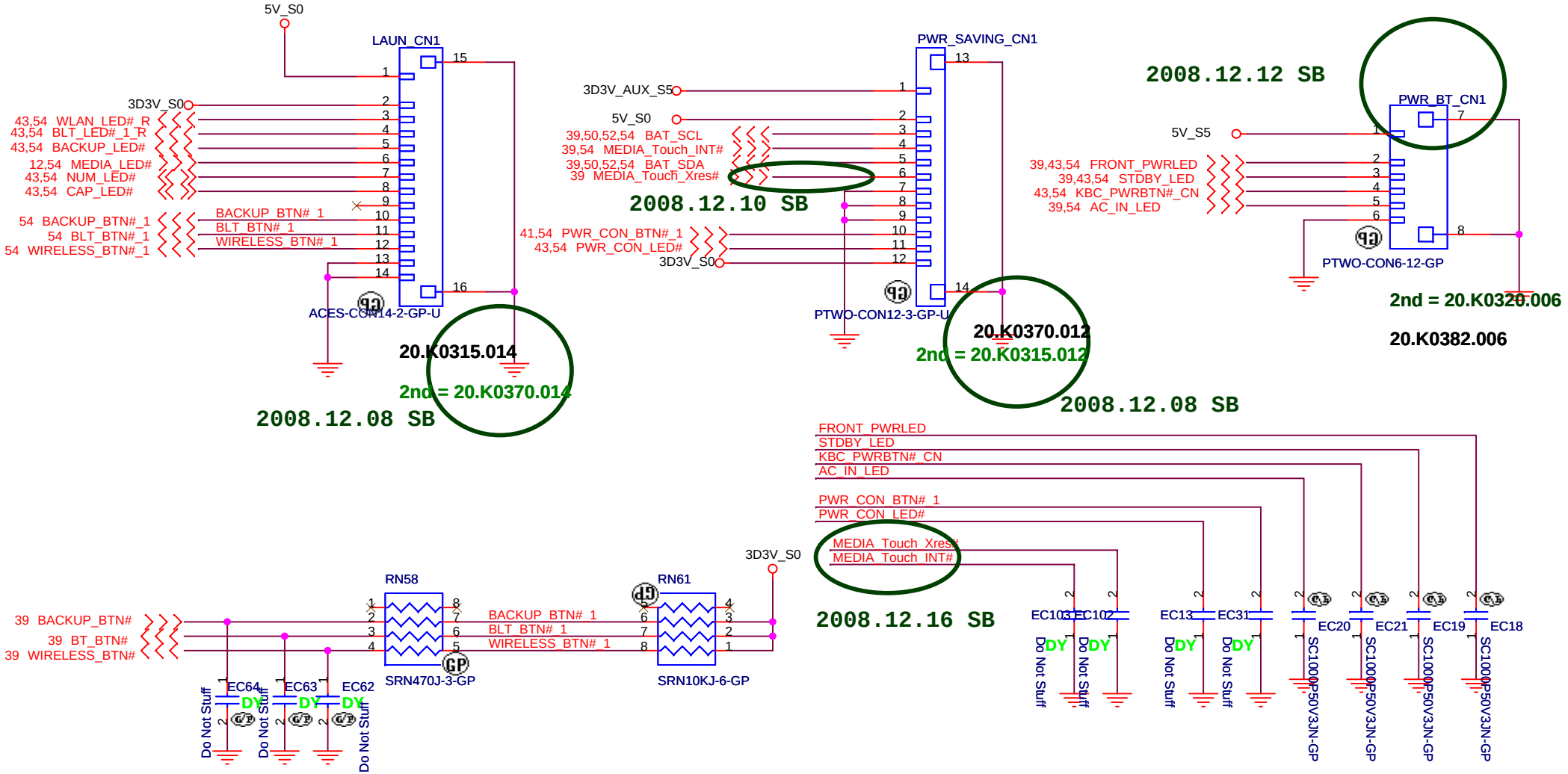
Date: Saturday, December 20, 2008	Sheet 41 of 55	



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Launch CN**

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A4	JM70-MV	SB

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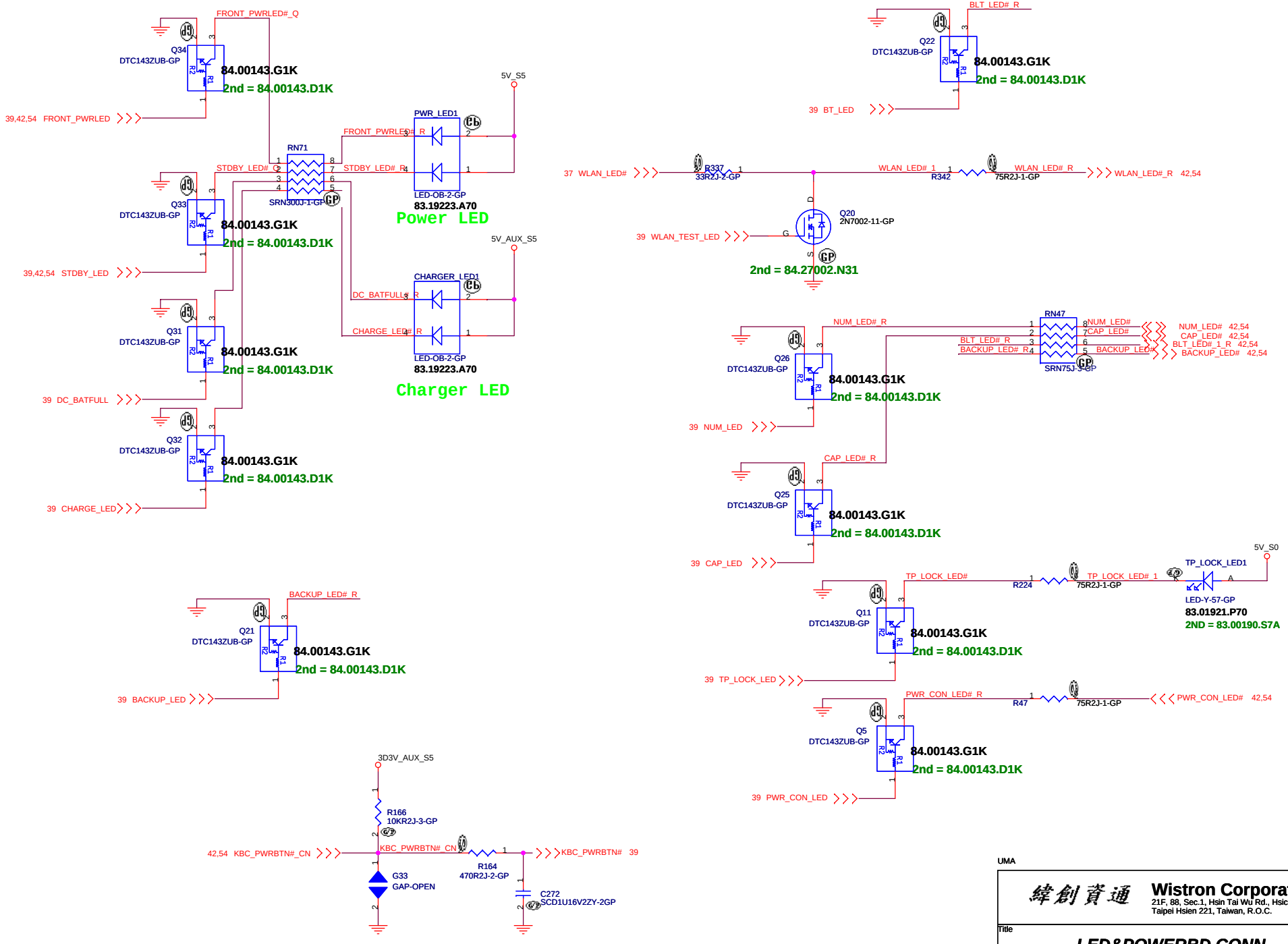
LED



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LED&POWERBD CONN***	
Size	Document Number **JM70-MV**	Rev SB
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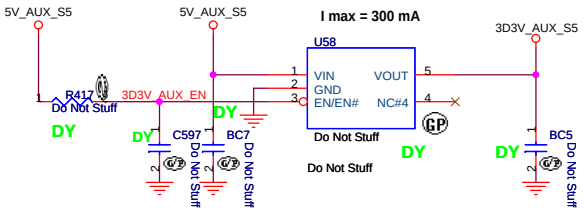
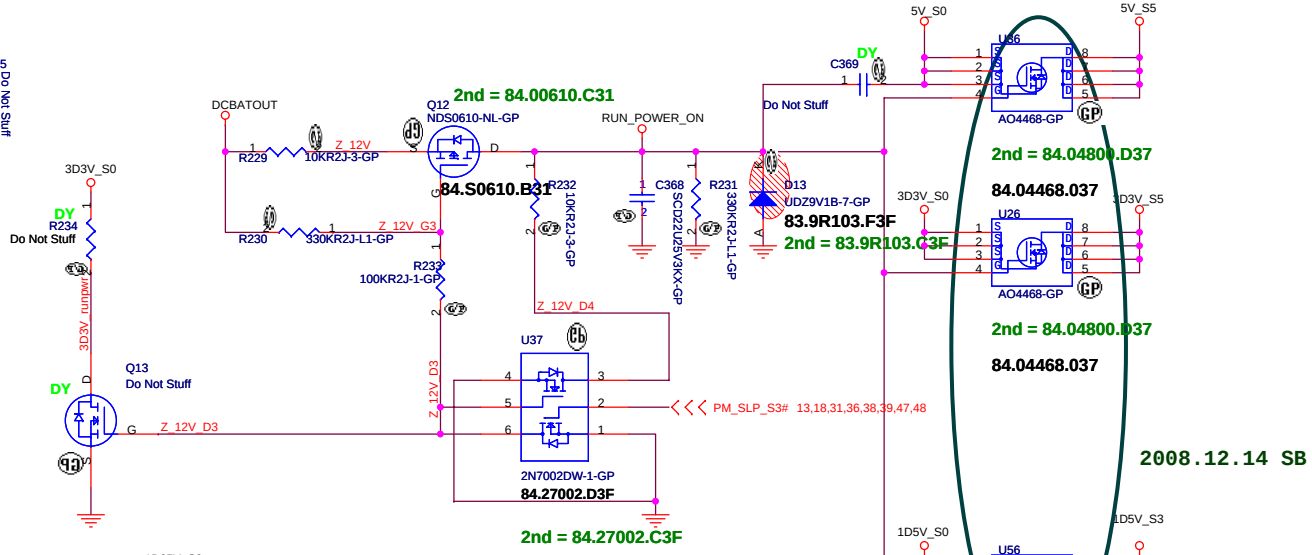
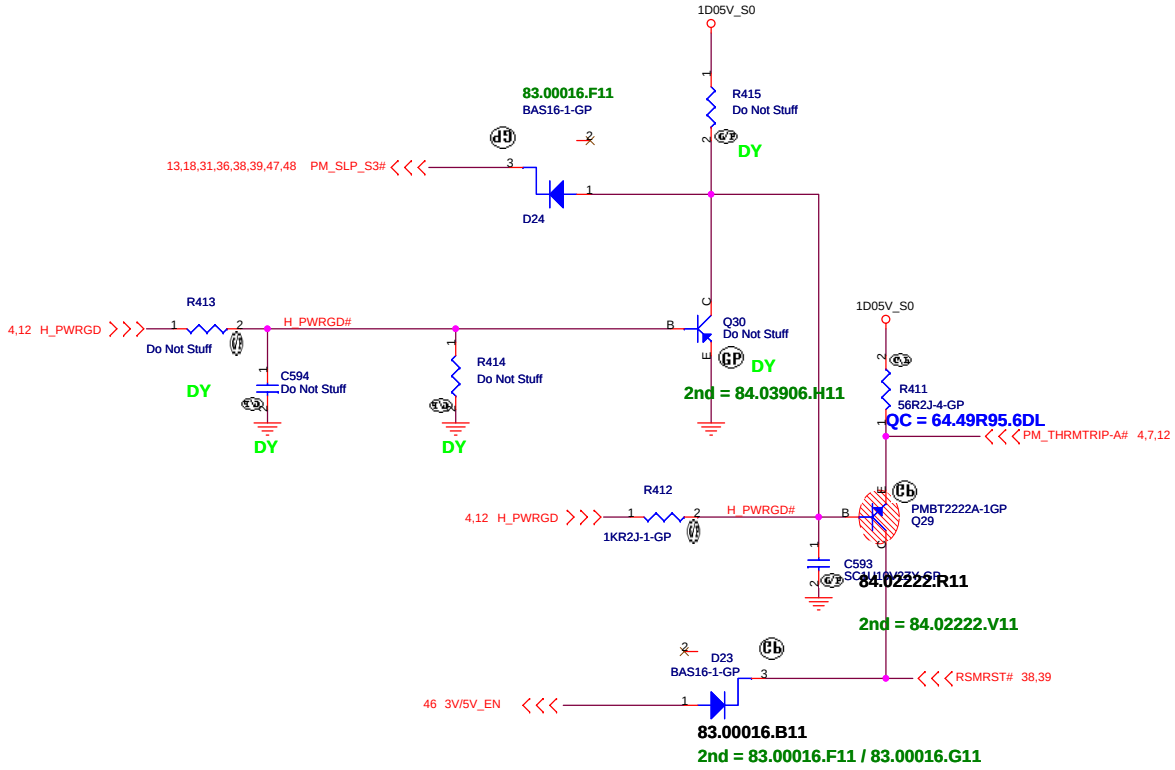
Aux Power

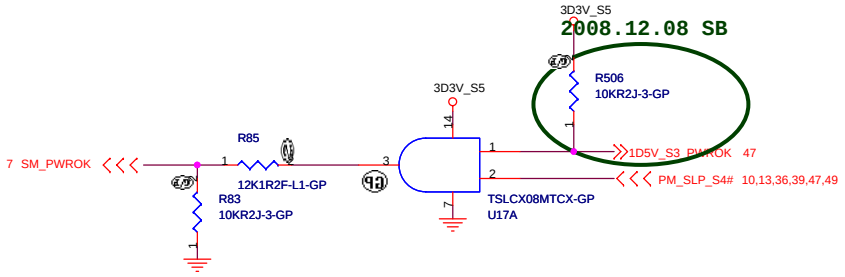
3D3V_AUX_S5



Run Power







UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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CPU_CORE
ADP3208C

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_VCORE
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

ISL62392
5V/3D3V

DCBATOUT_51125

PM_SLP_S4#

ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (7A)

DDR 3.0
RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
DDR_VREF_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON

VCC_GFXCORE(5.5A)

Charger ISL88731A

BATT_SENSE
AD+

Input Signal
FBS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

TPS51124
1D5V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D5V (O)
1D05V(O)

1D5V_S3 (10A)
1D05V_S0 (10.5A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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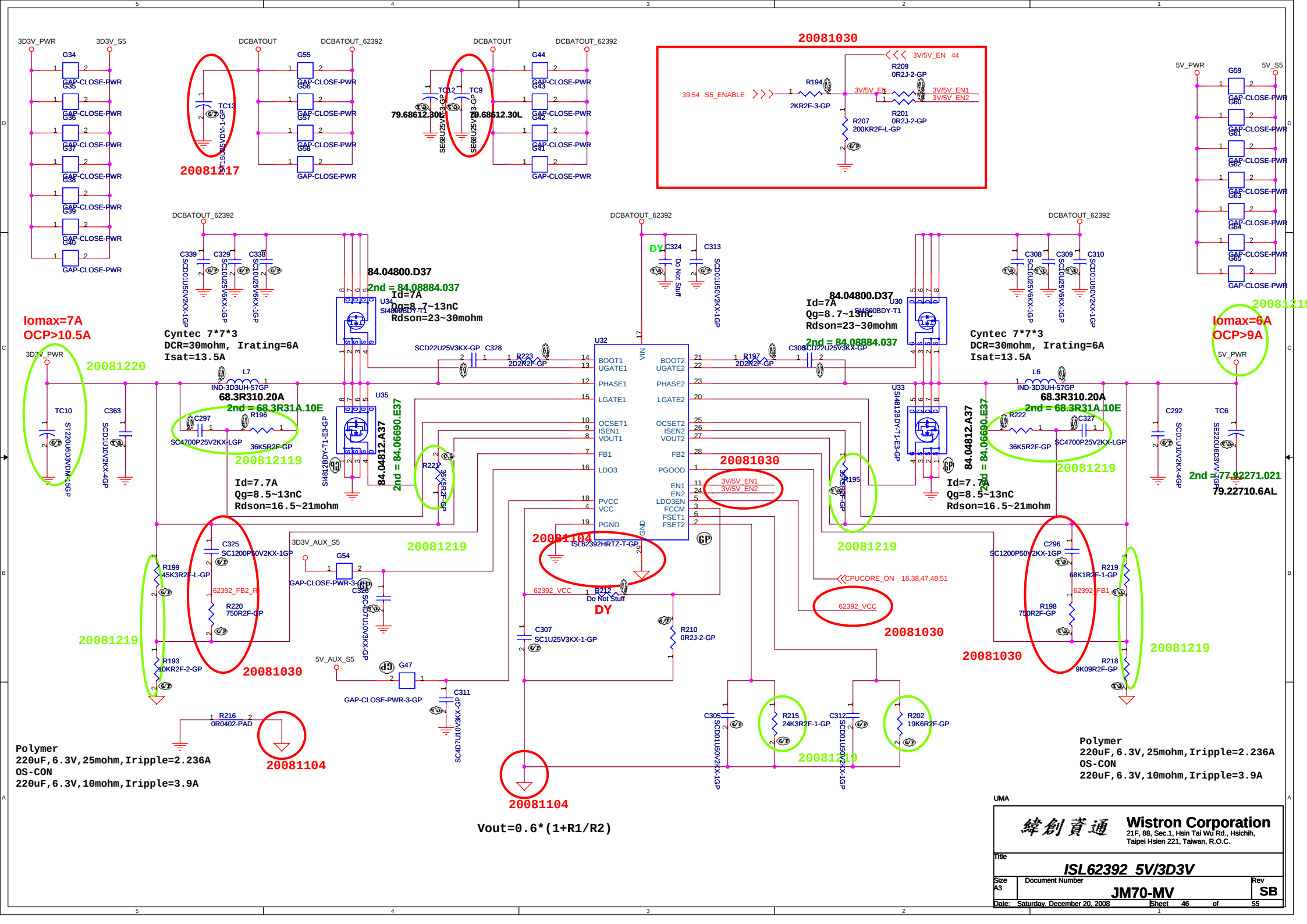
B	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 45 of 55


20081030
3V/5V_EN 44
R209 0R2J-2-GP
39,54 S5_ENABLE
R194 2KR2F-3-GP
3V/5V_EN
3V/5V_EN1
3V/5V_EN2
R201 0R2J-2-GP
R207 200KR2F-L-GP
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
DCBATOUT
DCBATOUT_62392
GAP-CLOSE-PWR
TC13 150U6D3VDM-1-GP
20081217
TC12 SE68U25VM-3-GP
TC9 SE68U25VM-3-GP
79.68612.30L
79.68612.30L
20081219
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
84.04800.D37
2nd = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U34 SI4800BDY-T1
U30 SI4800BDY-T1
DY
Do Not Stuff
C324
C313
SCD01U50V2KX-1GP
C308
C309
C310
SC10U25V6KX-1GP
20081220
TC10 ST220U6D3VDM-15GP
C363 SCD1U10V2KX-4GP
L7 IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R31A.10E
C297 SC4700P25V2KX-LGP
R196 36K5R2F-GP
200812119
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
U35 SI4812BDY-T1-E3-GP
84.04812.A37
2nd = 84.06690.E37
R222 36K5R2F-GP
U32 ISL62392HRTZ-T-GP
SCD22U25V3KX-GP C328
R223 2D2R2F-GP
R197 2D2R2F-GP
C306 SCD22U25V3KX-GP
BOOT1 UGATE1 PHASE1 LGATE1 OCSET1 ISEN1 VOUT1 FB1 LDO3 PVCC VCC PGND
BOOT2 UGATE2 PHASE2 LGATE2 OCSET2 ISEN2 VOUT2 FB2 PGOOD EN1 EN2 LDO3EN FCCM FSET1 FSET2 VIN GND
20081030
3V/5V_EN1
3V/5V_EN2
R195 36K5R2F-GP
20081104
ISL62392HRTZ-T-GP
20081219
CPUCORE_ON 18,38,47,48,51
62392_VCC
R212 Do Not Stuff
DY
20081030
R210 0R2J-2-GP
C307 SC1U25V3KX-1-GP
3D3V_AUX_S5
5V_AUX_S5
G54
G47
GAP-CLOSE-PWR-3-GP
C325 SC1200P50V2KX-1GP
R199 45K3R2F-L-GP
R220 750R2F-GP
62392_FB2_R
R193 10KR2F-2-GP
20081219
20081030
C326 SC47U10V3KX-GP
C311 SC47U10V3KX-GP
R216 0R0402-PAD
20081104
20081104
Vout=0.6*(1+R1/R2)
Iomax=6A
OCP>9A
L6 IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R31A.10E
R222 36K5R2F-GP
C327 SC4700P25V2KX-LGP
20081219
C292 SCD1U10V2KX-4GP
TC6 SE220U6D3VM-7GP
2nd = 77.92271.021
79.22710.6AL
84.04812.A37
2nd = 84.06690.E37
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
C296 SC1200P50V2KX-1GP
R219 68K1R2F-1-GP
R198 750R2F-GP
62392_FB1
R218 9K09R2F-GP
20081219
20081030
C305 SCD01U50V2KX-1GP
R215 24K3R2F-1-GP
C312 SCD01U50V2KX-1GP
R202 19K6R2F-GP
20081219
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size A3
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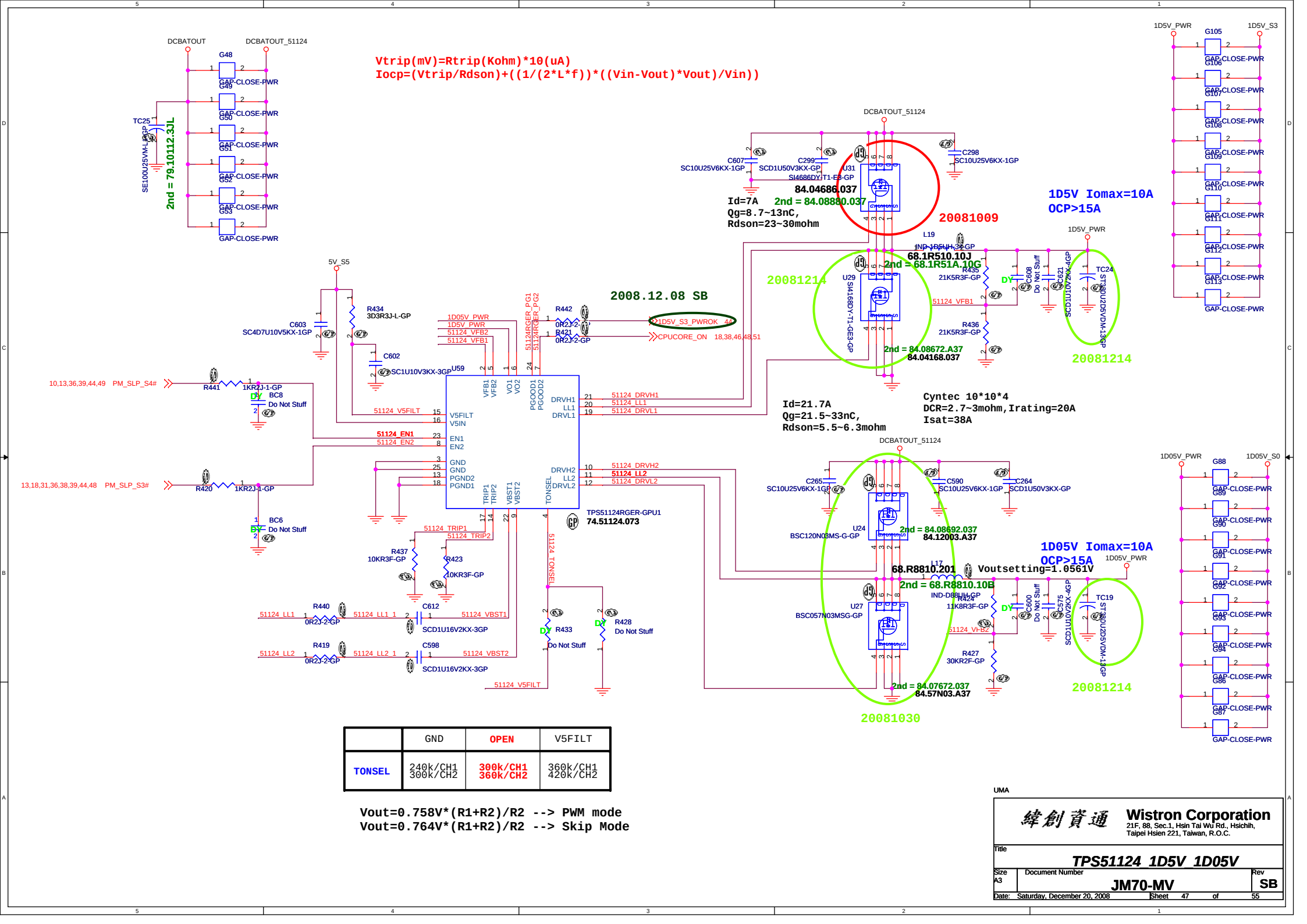

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D5V_1D05V

Size	Document Number	Rev
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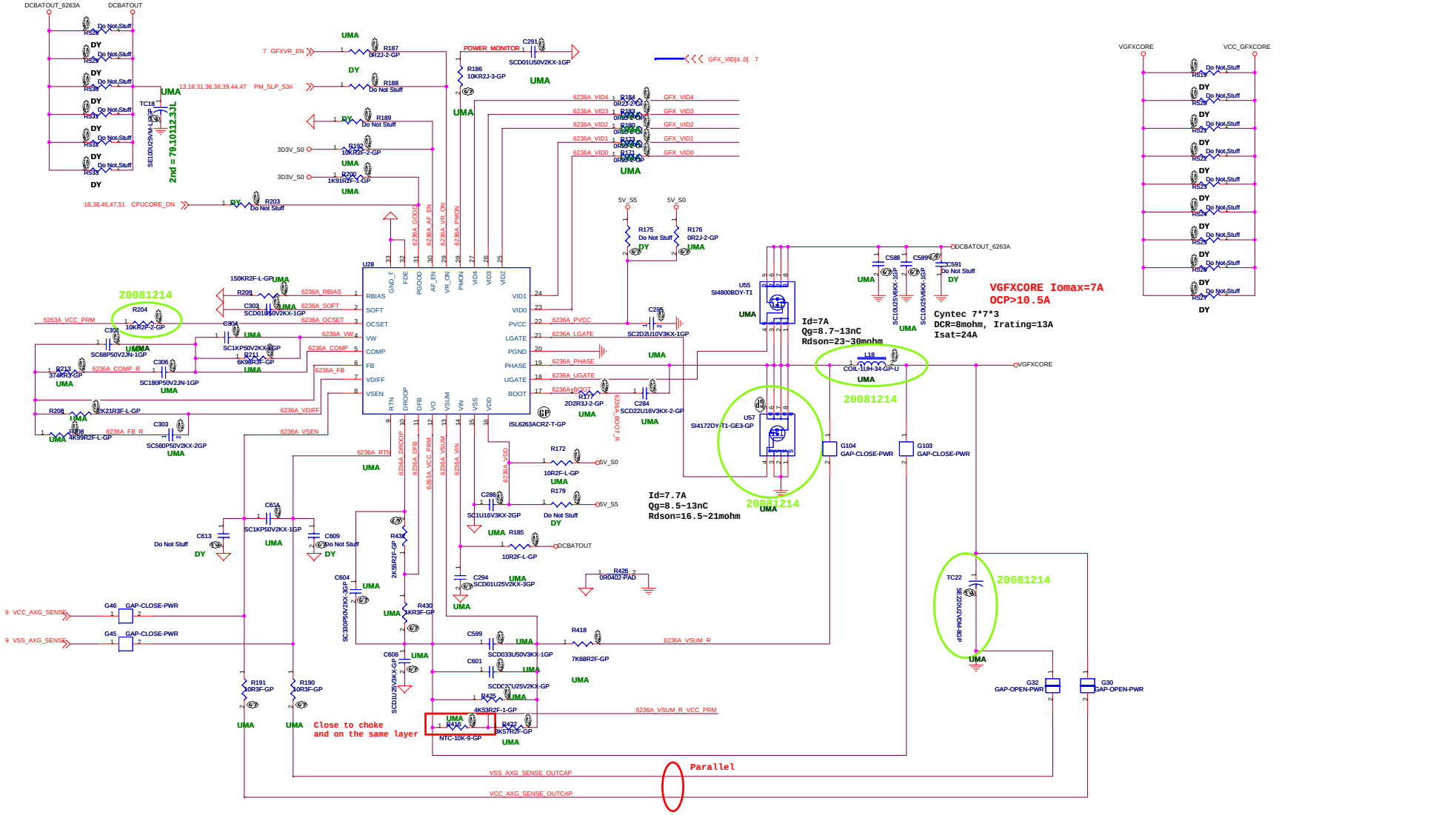
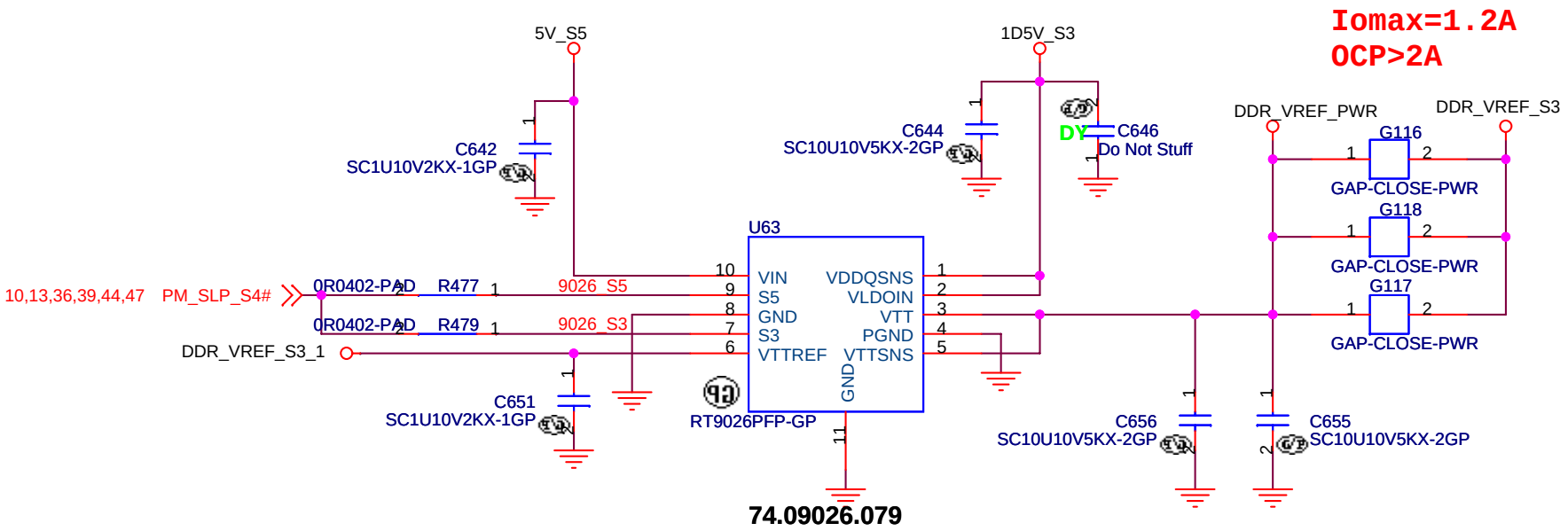


UMA

Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ISL6263A_GFX CORE			
Size: A2	Document Number: JM70-MV	Rev: SB	
Date: Saturday, December 20, 2008	Sheet 48 of 55		



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D75V

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A	JM70-MV	SB

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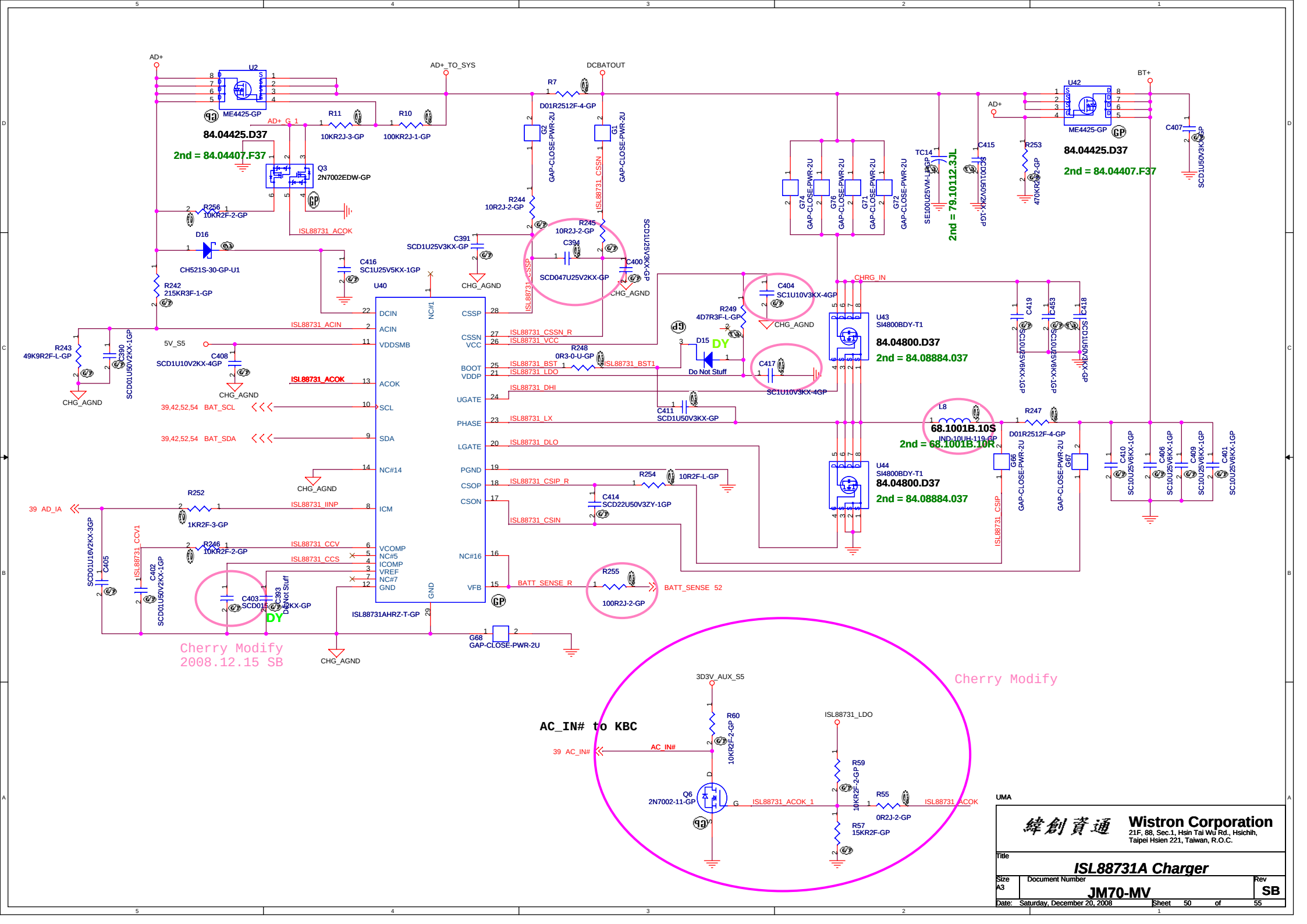
AD+
U2
ME4425-GP
84.04425.D37
2nd = 84.04407.F37
AD+_G_1
R11
10KR2J-3-GP
R10
100KR2J-1-GP
AD+_TO_SYS
DCBATOUT
R7
D01R2512F-4-GP
Q3
2N7002EDW-GP
R256
10KR2F-2-GP
ISL88731_ACOK
D16
CH521S-30-GP-U1
C416
SC1U25V5KX-1GP
R242
215KR3F-1-GP
U40
R244
10R2J-2-GP
R245
10R2J-2-GP
C391
SCD1U25V3KX-GP
C394
SCD047U25V2KX-GP
C400
SCD1U25V3KX-GP
ISL88731_CSSP
ISL88731_CSSN
G2
GAP-CLOSE-PWR-2U
G1
GAP-CLOSE-PWR-2U
CHG_AGND
R243
49K9R2F-L-GP
C390
SCD01U50V2KX-1GP
5V_S5
C408
SCD1U10V2KX-4GP
ISL88731_ACIN
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
39,42,52,54 BAT_SCL
39,42,52,54 BAT_SDA
39 AD_IA
R252
1KR2F-3-GP
R246
10KR2F-2-GP
C403
SCD015U16V2KX-GP
C393
Do Not Stuff
DY
C405
SCD01U16V2KX-3GP
C402
SCD01U50V2KX-1GP
ISL88731_CCV1
ISL88731_CCV
ISL88731_CCS
ISL88731_IINP
ISL88731_ACIN
ISL88731_VCC
ISL88731_CSSN_R
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
R248
0R3-0-U-GP
R254
10R2F-L-GP
C414
SCD22U50V3ZY-1GP
C411
SCD1U50V3KX-GP
R255
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 52
G68
GAP-CLOSE-PWR-2U
R249
4D7R3F-L-GP
D15
Do Not Stuff
C404
SC1U10V3KX-4GP
C417
SC1U10V3KX-4GP
CHRG_IN
U43
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
U44
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
L8
68.1001B.10S
IND-10UH-119-GP
2nd = 68.1001B.10R
R247
D01R2512F-4-GP
G66
GAP-CLOSE-PWR-2U
G67
GAP-CLOSE-PWR-2U
C419
SC1U25V6KX-1GP
C453
SC1U25V6KX-1GP
C418
SCD1U50V3KX-GP
C410
SC10U25V6KX-1GP
C406
SC10U25V6KX-1GP
C409
SC10U25V6KX-1GP
C401
SC10U25V6KX-1GP
BT+
U42
ME4425-GP
84.04425.D37
2nd = 84.04407.F37
C407
SCD1U50V3KX-GP
R253
470KR2J-2-GP
C415
SCD01U50V2KX-1GP
TC14
SE100U25VM-LGP
2nd = 79.10112.3JL
G74
G76
G71
G72
GAP-CLOSE-PWR-2U
Cherry Modify
2008.12.15 SB
AC_IN# to KBC
3D3V_AUX_S5
R60
10KR2F-2-GP
AC_IN#
39 AC_IN#
Q6
2N7002-11-GP
ISL88731_ACOK_1
R59
10KR2F-2-GP
R55
0R2J-2-GP
R57
15KR2F-GP
ISL88731_ACOK
Cherry Modify
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JM70-MV
Rev
SB
Date: Saturday, December 20, 2008
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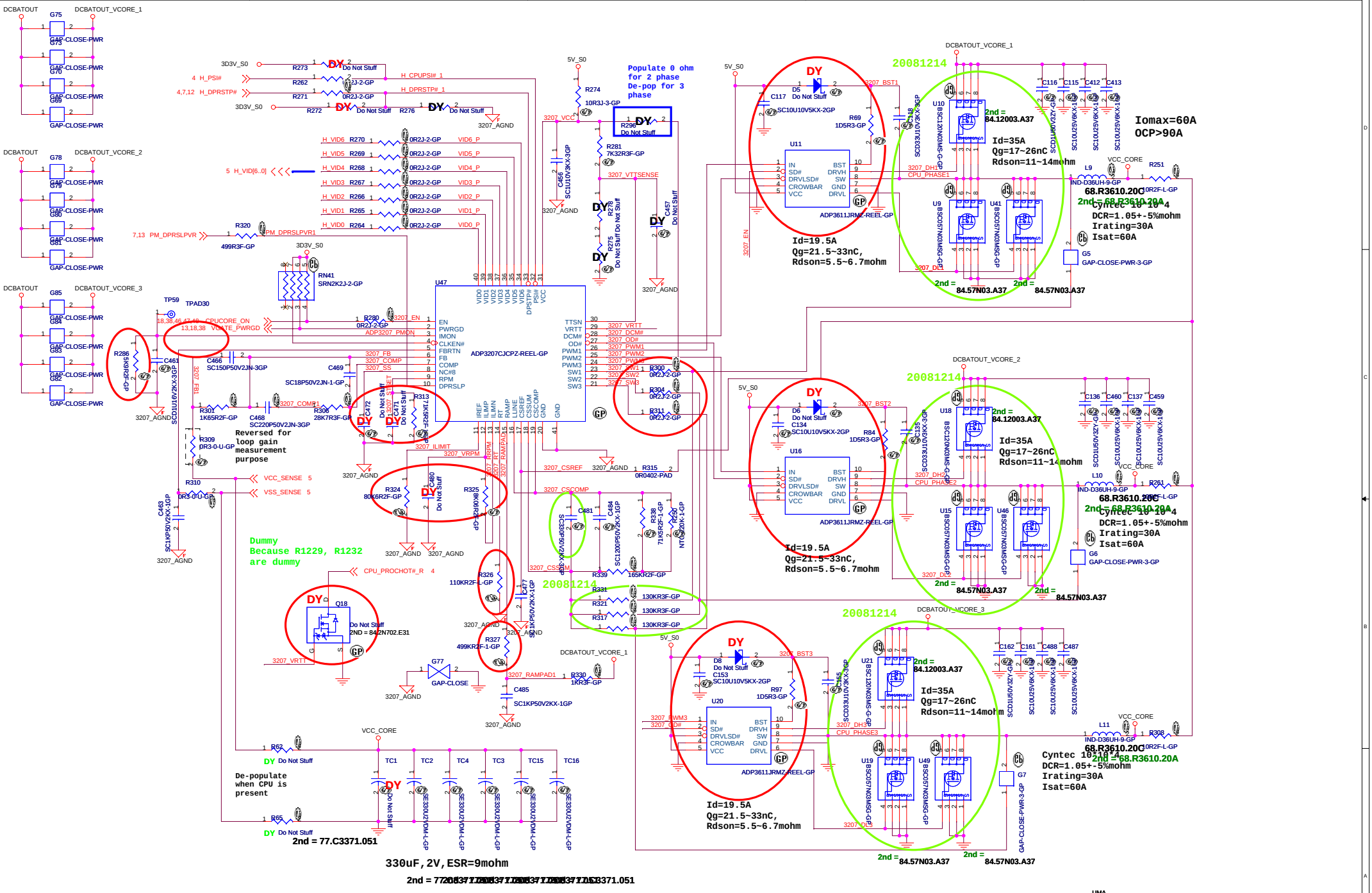
ADP3207C_CPU CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Size: Custom
Document Number: JM70-MV
Rev: SB
Date: Saturday, December 20, 2008
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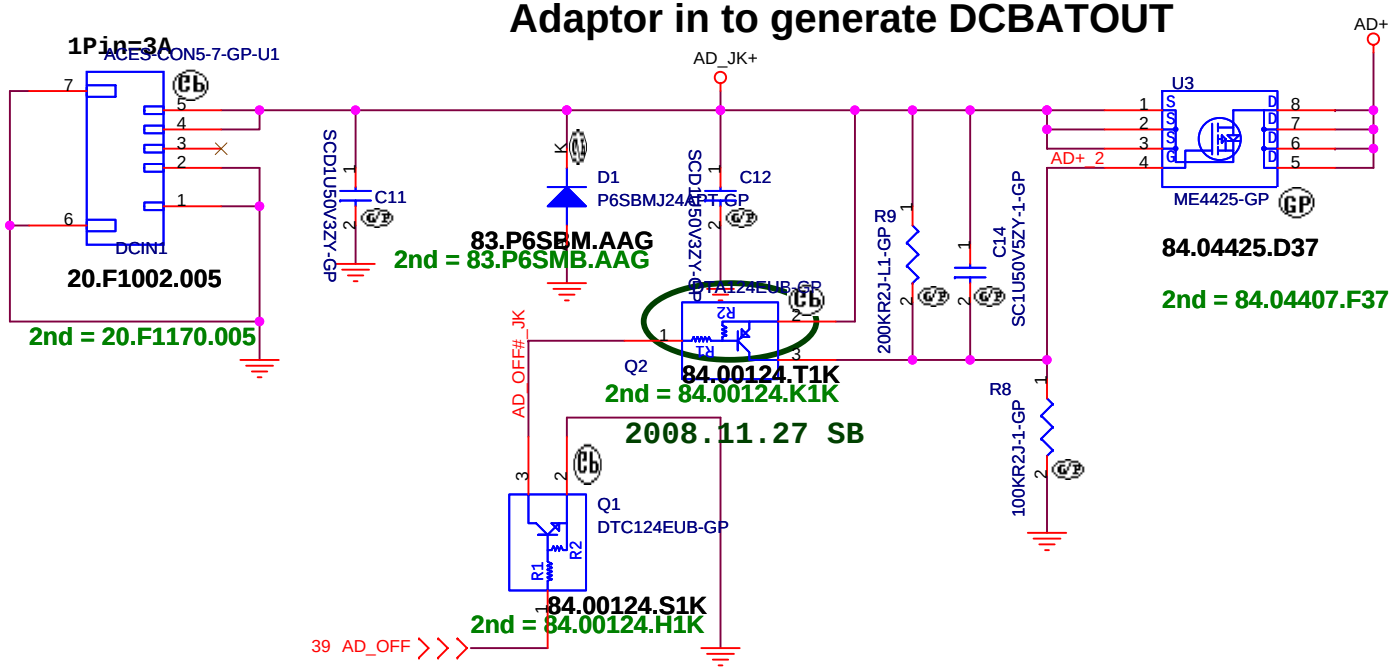
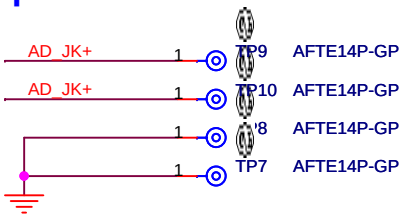
UMA
ADP3207CJCPZ-REEL-GP
ADP3611JRMZ-REEL-GP
20081214
Iomax=60A
OCP>90A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Cyntec 102104
DCR=1.05+-5%mohm
Irating=30A
Isat=60A
68.R3610.20C
2nd = 68.R3610.20A
Reversed for loop gain measurement purpose
Dummy
Because R1229, R1232 are dummy
De-populate when CPU is present
2nd = 77.C3371.051
330uF,2V,ESR=9mohm
Populate 0 ohm for 2 phase
De-pop for 3 phase
2nd = 84.12003.A37
2nd = 84.57N03.A37

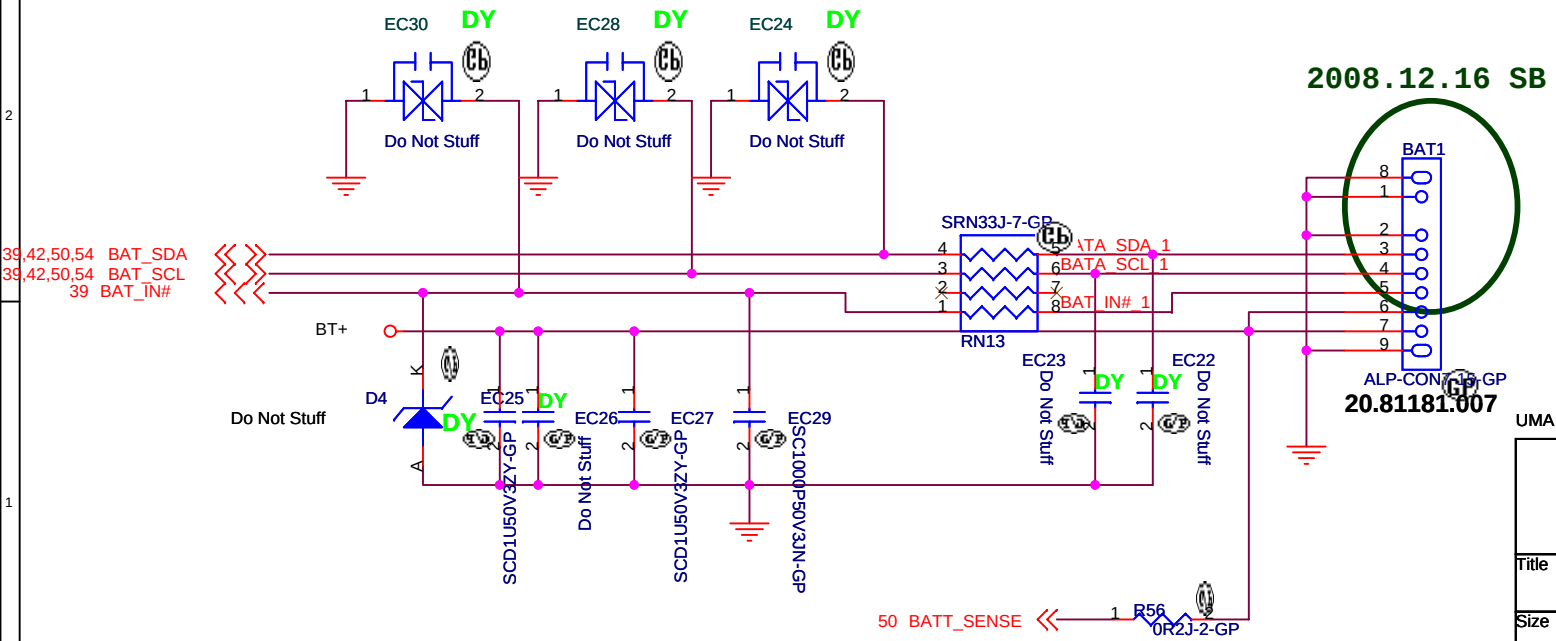
Adaptor in to generate DCBATOUT



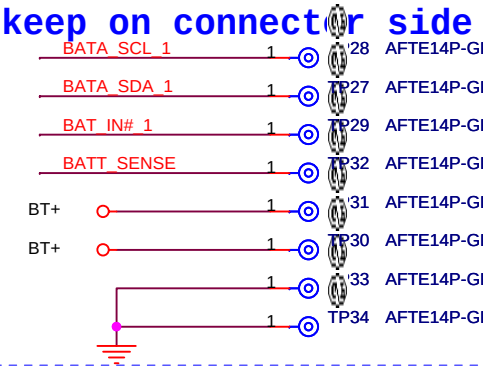
KB Conn. Test Point keep on connector side



MAIN BATTERY CONNECTOR



BAT1 Conn. Test Point keep on connector side



UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD&BTY CONNECTER**

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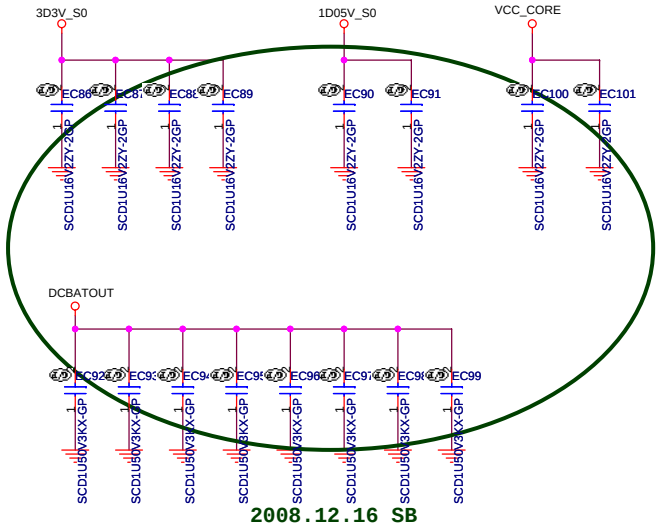

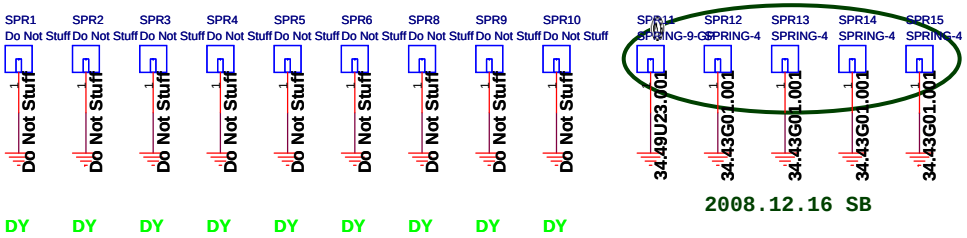

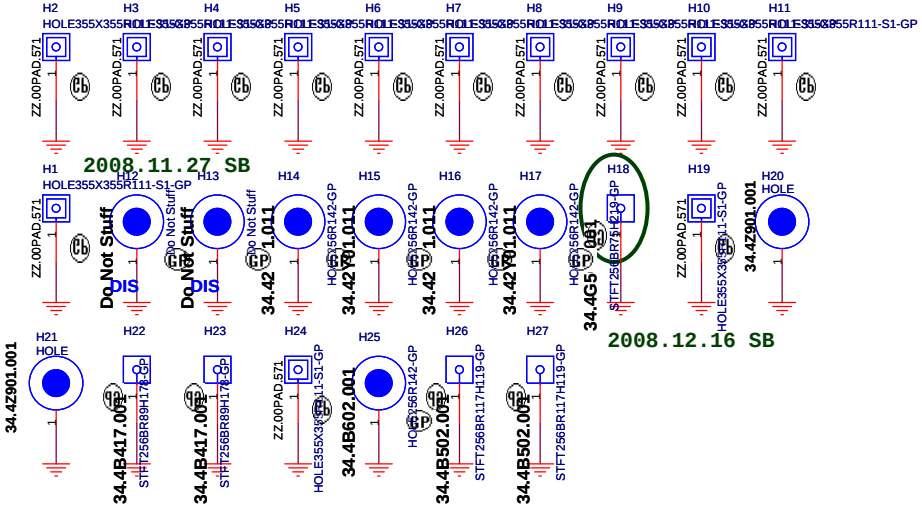

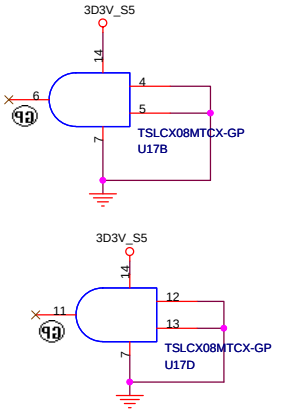

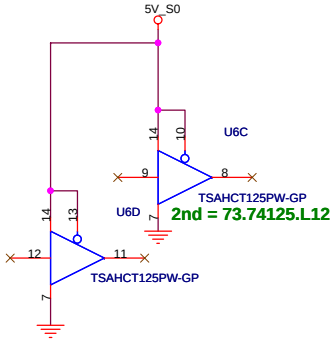

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***EMI/Spring/Boss***	
Size	Document Number **JM70-MV**	Rev SB
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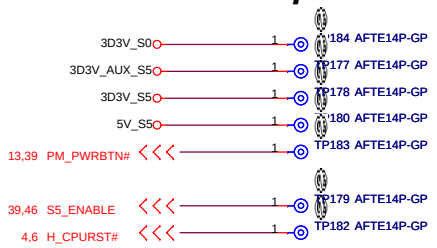
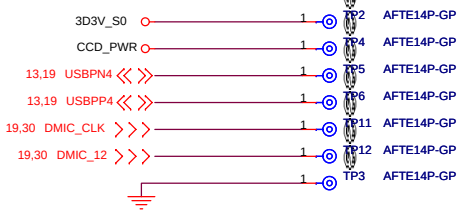
Check test point

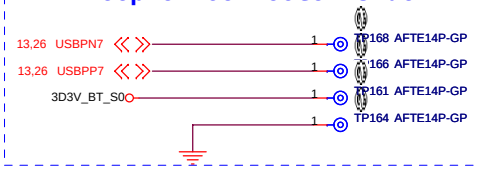


Test Point放在Dimm Door打開可量測處

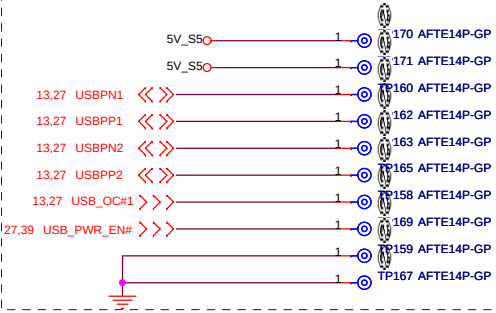
CCD_DMIC_CN1 Conn. Test Point keep on connector side



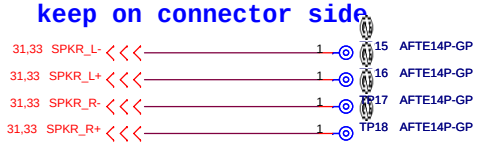
BT Conn. Test Point keep on connector side



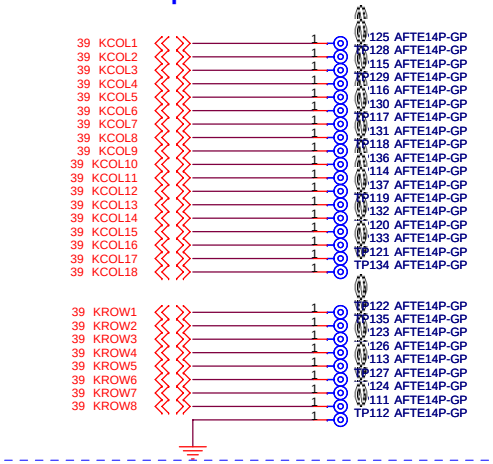
USB_CN1 Conn. Test Point keep on connector side



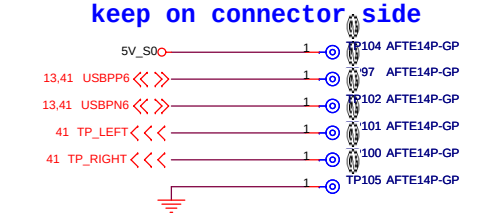
SPKR1 Conn. Test Point keep on connector side



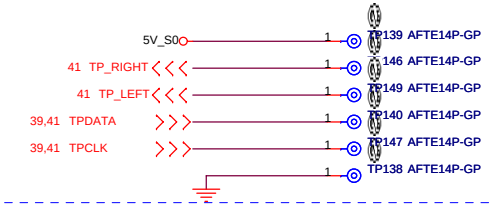
KB1 Conn. Test Point keep on connector side



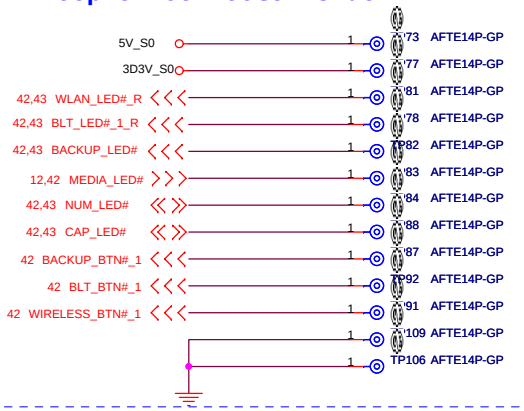
FP test Point keep on connector side



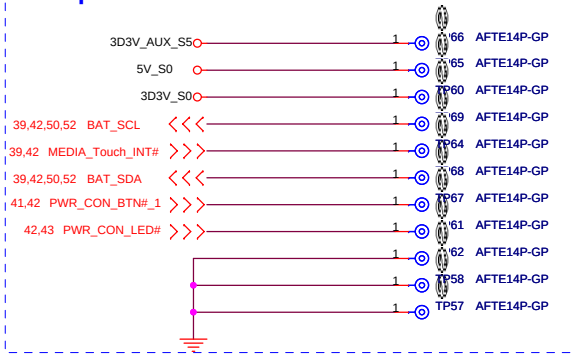
TOUCH PAD Conn. Test Point keep on connector side



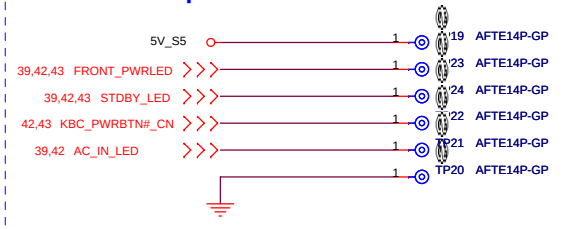
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side



PWR_BT_CN1 Conn. Test Point keep on connector side



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AFTE_TP

Size: A3 | Document Number: JM70-MV | Rev: SB

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UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

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